



**INTERNATIONAL JOURNAL OF NOVEL RESEARCH
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ISSN : 2456-4184

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Padala Jayakrishna Chary

In recognition of the publication of the paper entitled
Design of 16-bit Adder, Multiplier and ALU using Reversible Logic Gates

Published In IJNRD (www.ijnrd.org) ISSN Approved & 8.76 Impact Factor

Published in Volume 8 Issue 6, June-2023 | Date of Publication: 2023-06-10

Co-Authors - A. Lahari, A. Mahesh, G. Nagireddy



Research Through Innovation

Registration ID : 198667

Paper ID - IJNRD2306167

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