DESIGN OF RING OSCILLATOR BASED DDFS ALGORITHM & ARCHITECTURE BASED ON 0.18UM CMOS

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Abstract— This paper introduces a ring oscillator based novel DDFS technique for generation of fixed period synthesized output signal. Generally it is seen that DDFS designed using arithmetic circuits (Direct Analog) and loop based technique's (PLL/VCO) provides synthesized signals with instantaneously varying time periods from a fixed period input clock signal. This type of synthesized signals create a major bottleneck when used in sensitive & precise application due to its time varying nature which in turn puts tight constraints on reference clock, power supply and system noise. In the presented work a RO based complete digital block ASIC architecture has been designed in which properly modulated input clock signal from RO is utilized to obtain a fixed period synthesized output signal. Presented synthesizer can be suitably incorporated for design of low power & area constrained VLSI architectures or programmable low scale integration processes with incorporated wide bandwidth range & low power consumption . Simulation result justify the proposed algorithm's validity and its improvement in performance over arithmetic and loop based architecture's.

Keywords— ASIC, CMOS, Direct Digital Frequency Synthesis (DDFS), Frequency Synthesis, Ring Oscillator (RO)

I. INTRODUCTION

Frequency synthesizer can be explicitly defined as an electronic component which accepts a incoming reference frequency (f_{ref}) and generates a corresponding output frequency (f_{out}) as determined by the control word(f_c) [3][18]. In present commercial communication industry frequency translation has assumed a major role for frequency synthesizer with demand for synthesizers providing high resolution, wide bandwidth and fast switching speeds , with the scaling down of devices resulting in more compact arrangement , need for SoC chips has risen exponentially in recent years. Keeping in conformity with the moore's law more component are being tried to accommodate within lesser silicon area and with low power dissipation /consumption rating. ASIC design approach provides a ready solutions to some of the problems keeping in conformity with the above defined criterions.

Depending on the method incorporated for frequency generation frequency synthesizers are classified into three broad categories namely [3][18]

a. Phase-Locked loop (PLL) or " Indirect type " .
b. Mixer / filter / divide or " Direct analog type ".
c. Direct digital synthesis type.

Though the methods of frequency generation stated above provides its own set of advantages and disadvantages when applied for precise application specific purpose. Still now PLL method for frequency synthesis is being widely used in industry for frequency generation and synthesis purposes but the major hindrance encountered while using this method of frequency synthesis is that a wide frequency bandwidth and fast switching speed is difficult to achieve even with the application of aggressive PLL/VCO pretuning technique's. Similarly direct analog method for frequency synthesis utilizes conventional arithmetic blocks i.e multiplier, adder divider etc to produce desired synthesized output frequency. Being an expensive method for frequency synthesis direct analog method also encounters some fundamentals shortcomings as the process is completely oriented around implementation and utilization of analog blocks hence it inadvertently affects the power and area constraints[3]. Lastly direct digital synthesis which is the theme of this paper poses some advantages over the previously discussed methods for frequency synthesis. Direct digital synthesis method utilizes an array of logic and memory element for constructing the desired synthesized output signal and a D/A converter is used at the output end to convert the generated digital signal to corresponding analog value. But the use of D/A converter poses limitation to the efficiency of this method. Also the reference clock used to generate the fundamental frequency should always operate at a higher frequency compared to the desired synthesized output frequency keeping in conformity with the Nyquist theorem.

The paper is organized as follows, Section 2 gives a short insight into the previously carried out work in design & development of direct digital frequency synthesizers. Section 3 deals with the working principle of the proposed algorithm.. Section 4 deals with the experimental & simulation results of the proposed architecture. Section 5 provides a conclusion to the work carried out and its possible future modif

II. RELATED WORK

As reported by Hugh Mair & Lining Xiu [3] in their paper on high-performance of frequency & phase synthesis. Frequency synthesizers architecture capable of synthesis of a signal with varying frequencies & phase was presented. The objective of the proposed architecture was synthesis of signals having varying frequency components sourced from multiple reference inputs of same frequency but with different phases. In some instance it was found that the final synthesized output was time varying in nature. Moreover in order to attain a acceptable jitter performance, phase deviation of this synthesized signals needed to be well controlled.

Similarly a related work on frequency synthesizer was presented by Milan Stork [18] in this paper the author presented an improved architecture for frequency synthesis based digital building block which can be effectively utilized for frequency & phase synthesis purpose.

The circuit was primarily based on implementation of generators, counters & registers. But the proposed architecture's efficiency reduced while operating on low output frequencies.

A new ring oscillator based approach for direct digital frequency having an improved spectral purity was proposed by B.C Sarkar & M.K Mandal [1][2] in their paper. This proposed architectural algorithm put forward a novel method for generation of fixed period signals by implementing the modulation technique on the fundamental frequency sourced from the ring oscillator arrangement. This technique proposed a novel technique over the already available techniques for frequency and phase synthesis. But the success of the proposed technique depended solely of the circuit performance for modulation of the fundamental frequency generated by a predefined criterion & also on the performance of multi-stage ring oscillator. Thought the experiment was carried out in the lower end of the RF spectrum. But the authors proposed its possible implementation in the higher frequency spectrum with proper circuit modifications.

III. PRINCIPLES OF OPERATION

The simplified block diagram for complete digital frequency synthesis based on the proposed algorithm is presented in Fig 1.

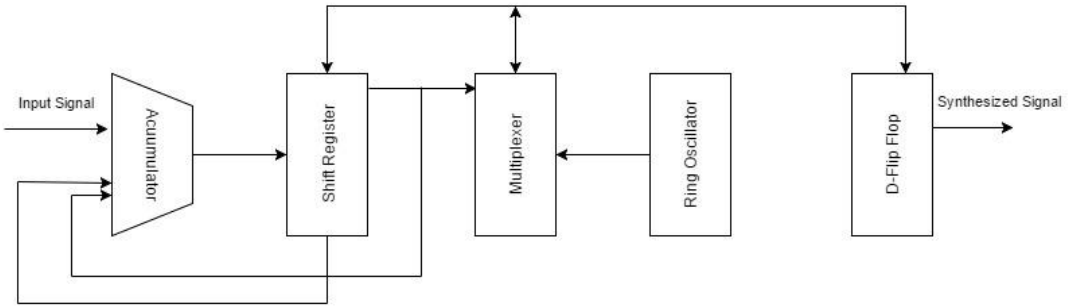

Fig 1. Block diagram for the proposed architecture

In the proposed block diagram as evident the incoming reference frequency bits are applied to MSB input terminals of the n-bit adder arrangement also referred as accumulator (ACC). Subsequently the output bits from the accumulator is applied to the input terminals of the n-bit shift register also referred as phase register (PR). A binary bit stream of data (k) normally consisting of (n-1) bits is summed up with the contents of the phase register keeping in conformity with timing period of (t_d) from the mentioned accumulator setup. 'T_d' is actually the period of shifting of clock pulse as applied to the phase register. The period of the synthesized signals as obtained from the MSB terminals of the phase register, can be mathematically equated as.

$$T = \left(2^n/_k\right) t_d \quad \text{..... (1)}$$

Here 'k' represents the binary bits from the output terminal of the accumulator. 't_d' represents the period of shifting of pulses from the clock, 'n' represents the n-bits of the accumulator.

ALGORITHM

In order to achieve the objective of selection for a particular shortened periodic pulse from a train of (c+1) pulses. The extent to which the periodic pulse should be reduced can be easily approximated from the content of the phase register (q) when the accumulator stack overflows releasing the excess bit in form of " carry out " pulse. The frequency control data of the accumulator (k) which is being supplied from the LSB terminals of the phase register the actual reduction of clock period (t_d) should be approximately $(q/k)t_d$. In order to vividly understand the working lets us assume that both the accumulator and the phase register are reset so in this condition overflow of bits will only take place when the sum of consequent bits tends to be equal to or more than 2^n thus triggering a new cycle for signal synthesis. Thus we can assume that the value of 2^n is equal to the total phase angle (φ) of a complete period

This means that the signal output has progressed by an amount of $(q/k)t_d$ at the beginning of a new cycle. So in order to cancel this increment in the content of the phase register the following remedial steps are taken.

i. One period of clock signal in every (c+1) bits of pulse train should be properly modulated by $(q/k)t_d$.

ii. The phase register should be reset for obtaining an overflow condition in form of "carry-out" phase in accumulator for (c+1)th perod of clock pulse

Following this above mentioned steps ensures purity of the the synthesized signal.

DESIGN

The digital block set for this proposed architecture has been designed keeping in conformity with the full custom design approach & BiSIM model for CMOS. Very important component in this proposed architectural algorithm for frequency synthesis is ring oscillator (RO) which functions as a fundamental frequency generator unit for the operation of the entire digital block set. In this algorithm a 15 stage ring oscillator, arranged in cascaded formation with delay stages in a closed loop feedback chain has been implemented using CMOS inverters with balanced transconductance parameters and this phenomenon has been kept prevalent in designing other components (i.e adder, shift register etc). Balancing of transconductance parameter is guided by the following mathematical equation

$$\left(^{Wp}/_{Lp}\right) = 2.5\left(^{Wn}/_{Ln}\right) \text{..... (2)}$$

Here W and L represents the width and length of the CMOS with annotations retaining their usual significance The propagation delay per stage (r_d) of the CMOS inverter depends on the propagation delay per stage and number of stages implemented to obtain self-sustained oscillation. The outputs branched from each stage can be easily combined to obtain multiphase clock signals. In a m-stage ring oscillator

structure each stage provides a phase shift of (π/m) and rest is provided by dc inversion. Below figure() shows a 5-stage CMOS ring oscillator which is scaled up by a factor of 3 in the actual design.

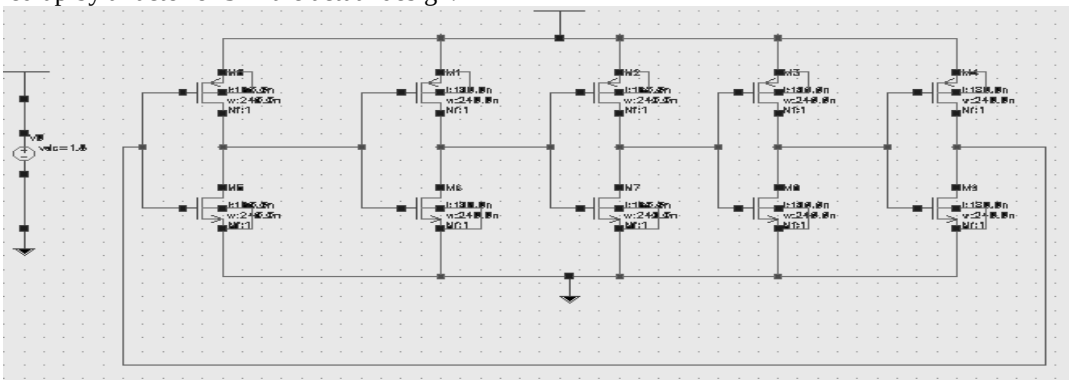

Fig 2: Shows a 5-stage ring oscillator structure

The pulse period obtained from the oscillator is discretely modulated through the multiplexer. The multiplexer selects a properly phase advanced pulse of ring oscillator from (m) branched outputs at the end of every inverter stage with odd and even numbered terminals. A specially designed circuits helps the multiplexer in selection process. The ring oscillator is basically 'm' odd number inverter stages. This (m) number of odd stages provide a 'm' square wave signals of equally spaced time period (t_d) which differs in its phase. The phase difference between two appropriately chosen signal is (2πi/m), where 'i' is an integer value in the range of 1 to (m-1). Any of this (m) signals generated can be appropriately chosen by the multiplexer. The inputs to the multiplexer are designed such that the outputs of the multiplexer for two consecutive selection word differ by a phase of (2π/m). This stated fundamental is applied in the multiplexer by applying alternate outputs of the ring oscillator (i.e even & odd) to inputs terminals of the multiplexer in a defined sequence. The even numbered outputs of the ring oscillator are LSB input terminals of the multiplexer and odd numbered outputs are applied to the MSB input terminals. Fig 3 shows the block diagram representation of the stated principle

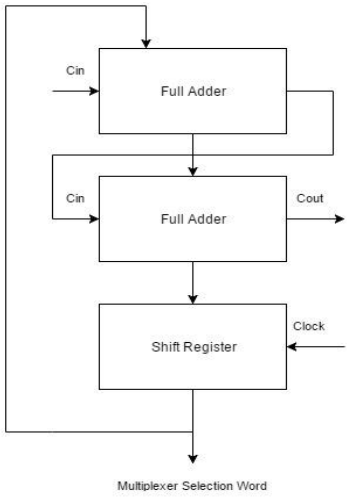

Fig 3: Shows the digital circuit for generating MUX selection word

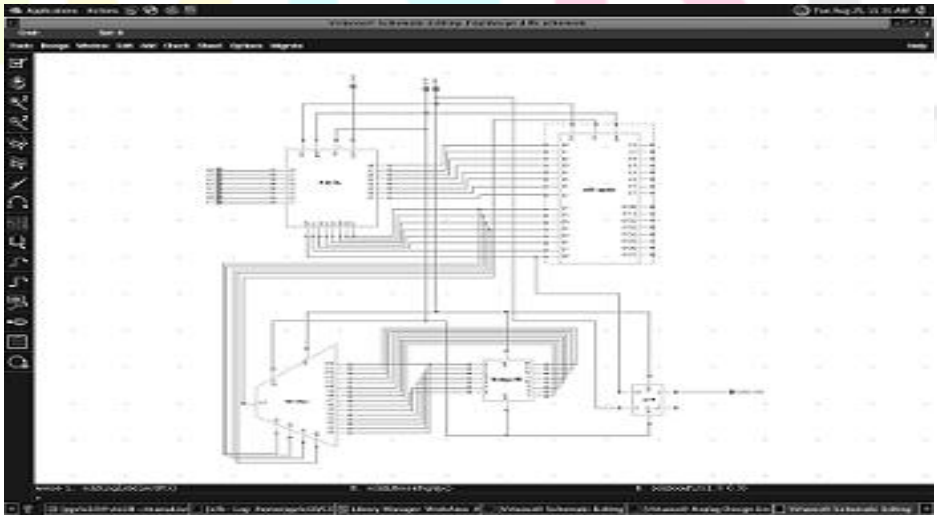

Fig 4: Logic circuit for the proposed ASIC.

The multiplexer selection word (SW) consist of 'p' bits such that ($p <= \log_2 m$) and it is chosen depending on the value of phase register at the instant when the overflow condition occurs in the accumulator.

The proposed algorithm states that at any instant of time the fundamental clock period should be reduced by a factor $(q/k)t_d$ which is equivalent to the corresponding phase change by $(2\pi/m)$. A logic circuit designed with a n-bit full adder and n-bit shift register determines the proper selection word for the multiplexer.

IV. SIMULATION

SEMICONDUCTOR PROCESS

The Full custom Design of the proposed frequency synthesizer architecture has been modeled using 180nm node technology and simulated in analog design environment (ADE-L) of cadence virtuoso IC design suite and simulated using SpectreS simulator . The entire architectural design is based on BiSIM model (version-3.3) for CMOS .Supply voltage of 1.8V was applied for simulating the designed architecture. The operating temperature range was chosen to be ambient temperature condition of 27^{o}C though it has been tested for its functional output based on military operation temperature range i.e -55^{o}C to 125^{o}C using corner analysis approach. The layout of the proposed architecture has been carried out in microwind layout editor with suitable verification.

TIMIMG CIRCUIT

Without the loss of generality the following values have been implemented during the simulation of the proposed architecture: m=15, p= 4, 8-bit accumulator, 16:1 multiplexer, 8-bit shift register. Figure 5 shows the transient analysis of the 15-stage ring oscillator outputs having consecutive output phases.

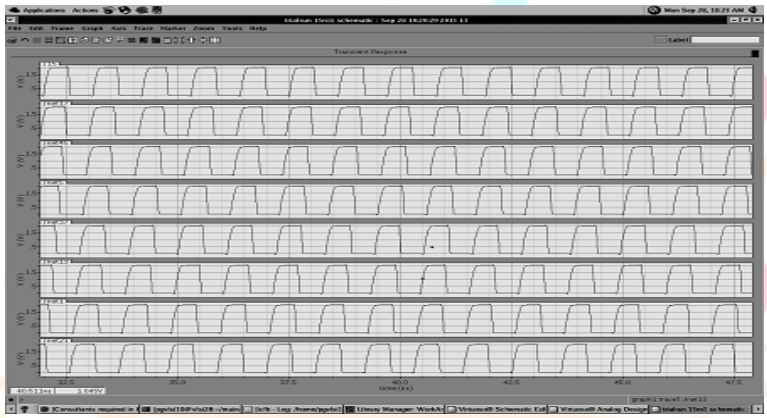

Fig 5: Transient analysis of the 15-stage CMOS ring oscillator

These generated signals from the ring oscillator are applied to the multiplexer input terminals in defined sequence. Analysis has been carried out by interchanging the values for 'k' and spectrum of the synthesized signals have been obtained. Figure 6 shows the transient analysis of the fundamental clock generator (i.e ring oscillator) used and correspondingly generated synthesized signal.

The figure below shows the transient response of the synthesized signal. The shortened pulse period of one cycle in every four consecutive pulse cycle can be observed from the figure and fixed period output signal is also evident.

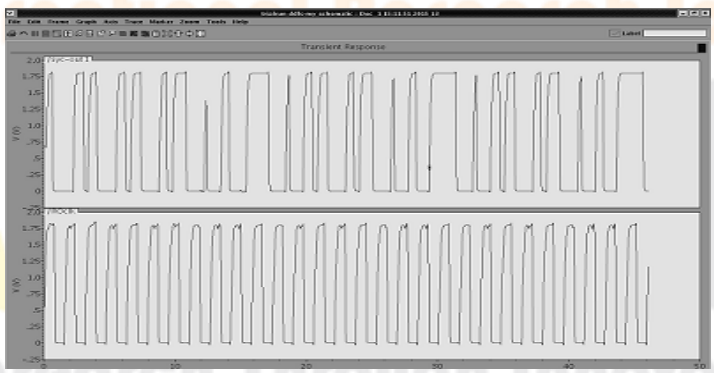

Fig 6: Transient response of proposed DDFS

The post layout simulation of the proposed algorithm has been carried on spectreS simulator and the result obtained is shown in figure 8 below

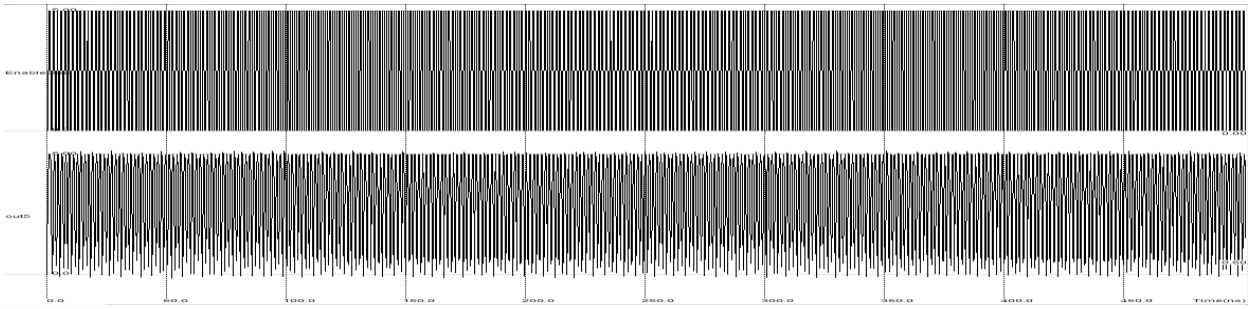

Fig 8: Shows the post layout simulation of the proposed ASIC architecture, the upper portion of the figure refers to the incoming signal and the below part depicts the generated synthesized signal

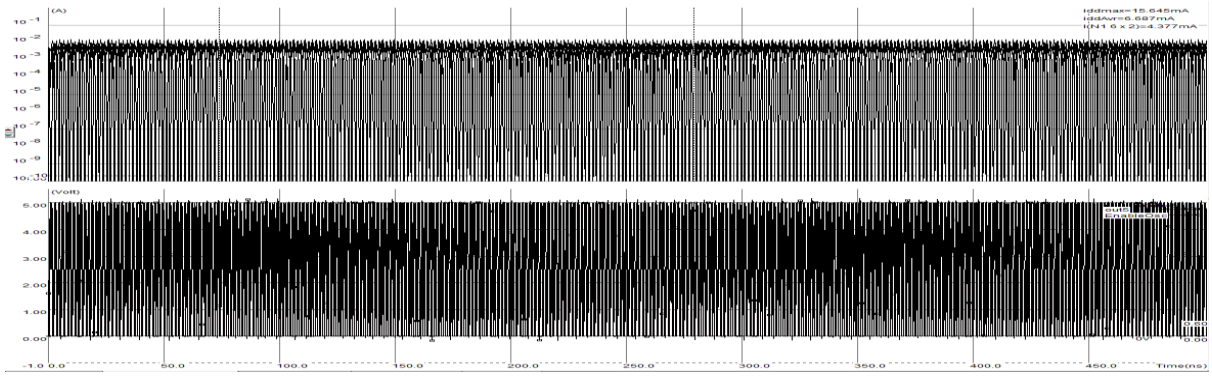

Fig 9: Shows a post layout current versus voltage plot of the proposed ASIC architecture

The layout of the proposed DDFS is area efficient as well as it consumes low power as compared to other reported architecture's. The dimensional and power consumption of the proposed layout has been given in the tabular form. The parametric details of the proposed layout is provided in table 1.

PROCESS	0.18 µm , 1.8V CMOS
Area (RO)	15mm^2
Area (DDFS)	0.49mm^2
Power Dissipation (RO)	28.5mW
Power Dissipation (DDFS)	544 mW
Output Frequency Range	1Ghz to 6.42 Ghz

Table 1: Parametric details of the designed ASIC layout

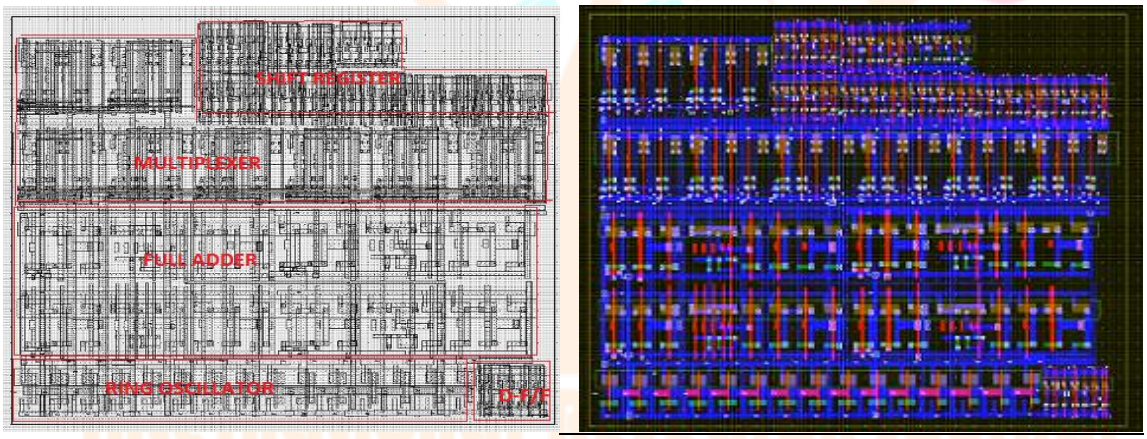

Fig 7: (a) Layout architecture in details (b) Layout of the proposed ASIC

PHASE & JITTER NOISE

Measurements related to noise performances are considered as an important parameter for characterization of timing circuits in modern digital logics. Noise parameters in digital domain is usually expressed in phase noise for frequency domain and jitter noise for time domain. Both terms represents a periodic signals deviation from their ideal signal in their respective domain.

A predictive logarithmic spectral density plot for a free running oscillator is provided in fig 10. Incase of a fundamental oscillator, noise generated is basically divided into two distinct regions, one indicating up-converted flicker noise. Up conversion is a result of modulation by the carrier signal. Flicker noise lies at 10dB/decade in a typical spectral density plot. When the noise is subjected to up-conversion then it is characterized by spectral density of oscillator lying at 30 dB/decade. It is represented by (1/f) as it is inversely proportional to the offset frequency of the carrier

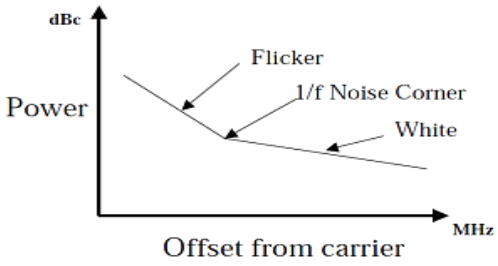

Fig 10: Spectral density representation of free running oscillator

Jitter is represented as time domain measurement of noise. Jitter refers to the deviation between expected cycle time with respect to time the signal actually takes to complete a cycle.The deviation from of a signal from its ideal form is depicted in the figure 11

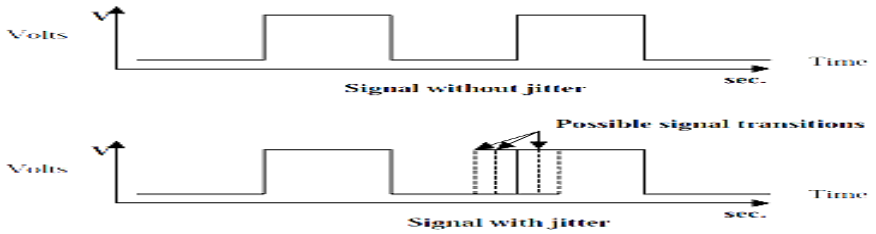

Fig 11: Deviation of original signal from ideal signal

Table below shows a comparative study of transient noise of different oscillator architectures

Oscillator Variant	Cycle jitter without supply noise(sec)	Cycle jitter with supply noise(sec)	Output voltage swing (volts)	Frequency dependence on supply voltage (Mhz/Volt)
Colpitts	5.85E-15	3.41E-12	5.95	25.5
Hartley	3.00E-14	4.50E-12	1.47	38.5
Delay Line	1.40E-14	3.50E-12	0.50	25.3
Ring	2.22E-13	1.30E-11	1.48	103
Active Inductor	1.30E-12	3.50E-11	0.21	450

Table 2: Shows a comparative study for cycle jitter for different class of oscillator

Generally it has been observed that oscillators employing passive elements in this architecture are less prone to jitter noise. As we can see that colpitts has the lowest cycle jitter. Though the ring oscillator used in the proposed algorithm as a fundamental clock in the proposed algorithm is susceptible to as compared to this passive counter parts but the main advantage offered by ring oscillator architecture over its counterpart is that it can be easily implemented in sub-micron MOS technologies as also consumes less power and area while implementation.

V. CONCLUSION

The effective implementation of the proposed design algorithm solely relies on the performance of the designed circuitry. The algorithm proposed in this paper is capable of reduction of clock pulse by a suitable amount. Another major factor on which the performance of the proposed frequency synthesizer architecture depends is on the performance m-stage ring oscillator designed using 'm' number of cmos inverter gates connected in a cascaded fashion. During simulation phases it was noticed that that value of 'k' heavily depends on the number of inverter stages in the ring oscillator. Also the reduction of the periodic pulses in the algorithm takes place in a discrete fashion which might also pose. a threat of obtaining erroneous results. Though the simulations have been carried out neglecting the jitter noise performance in its initial stages. But a further modification and analysis on the noise performance will be carried out in its advanced stages of development.

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