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Digital Modulation/Demodulation Techniques on FPGA

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Abstract : This paper presents an implementation of digital modulation/demodulation techniques on a field programmable gate array (FPGA), especially used for wireless communication. BASK, BFSK, BPSK and QPSK modulation and demodulation blocks have been implemented by multiplexer logic unit. Carrier signal has been generated by PWM technique rather than ADC/mega-wizard function available in Altera max Quartus software. As a reconfigurable hardware platform, Altera DE-1 cyclone-II family FPGA development and education board has been used. A brief description of theoretical aspects of the BASK, BFSK, BPSK and QPSK modulation and demodulation are covered.. FPGA implementation shows minimum number of logic modules(LMs) utilization within a chip. FPGA based modulation and demodulation is simpler and faster as well as it avoids high production cost, provides flexibility and adaptability with optimal power consumption.

IndexTerms **- binary amplitude-shift keying (bask), binary frequency shift keying (BFSK), binary phase-shift keying (BPSK), quadrature phase shift key(QPSK), MOdulator-DEModulator (MODEM), field programmable gate-array (FPGA).**

I. INTRODUCTION

Software Defined Radio(SDR) is an advanced communication system, significantly used for military and cell phone services. It is a collection of hardware and software where some or all of the radio's operating functions (also referred to as physical layer processing) are implemented through software. The implementation of Radio on programmable logic device not only improves area, speed and power but also easy to incorporate any advancement or modification in technique or technology due to its reprogrammable/reconfigurable features.

Use of FPGA in communication field is increasing progressively[1], since it can be easily programmed to the desired application or functionality requirements. It even allows designers to change their designs very late in the design cycle, even after the end of production and deployed in the field [2,3,11]. Different types of digital modulation techniques are developed for mobile communication system in order to procure higher data rate and to utilize limited spectrum efficiently[4]. At the same time, if small size and low power dissipation will be achieved by somehow either by using FPGA or ASIC, then system performance will be tremendously improved.

There are various modulation techniques used such as Binary Amplitude Shift keying(BASK), Binary Frequency Shift keying(BFSK) [5], and Binary Phase Shift keying(BPSK) to satisfy these requirements [6]. Binary Phase shift keying(BPSK) modulation technique is widely used because of its bandwidth efficiency and can be made power efficient with different modifications [8,9].

The objective of this paper is to implement BASK, BPSK, BFSK and QPSK digital modem(modulation- demodulation) on FPGA. This work employs the minimum number of blocks for achieving these four modulation techniques in an easy way [10,11]. Modulation blocks are basically realizing from multiplexer logic unit and Demodulation blocks are from comparator and AND gate logic. High frequency carrier has been generated by Pulse Width Modulation(PWM)[2] technique in which the inbuilt clock oscillator of 24/27/50 MHz on FPGA board has been used. Low Pass Filter(LPF) has been implemented on breadboard for Sine/Cos signal from PWM signal.

The paper is organized as follows. In Section II, the basic theory on Digital Modulations techniques have been discussed. In Section III, implementation on Altera's DE1 FPGA has been explained and post-implemenation results have been shown in section IV. Finally, in Section V, conclusions have been drawn.

II. BASIC THEORY

In Binary Amplitude-Shift Key(BASK) modulation process[5], the sinusoidal carrier signal will be present when information signal, which is in the digital form, has logic high ('1') and absent when it has logic low ('0'). The frequency and phase of the carrier signal will be remain constant, as shown in **figure 1**. In order to achieve this functionality, 2:1 multiplexer is used as shown

in **figure 2**. **Figure 3** shows demodulation process for BASK signal. The received BASK signal will be rectified, then pass through the filter to eliminate high frequency carrier. The comparator compares the output signal from LPF with reference signal and generates digital information signal which found same as transmitted one[3,5].

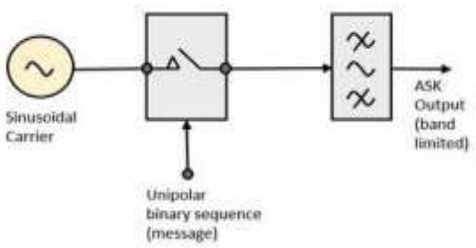


Figure 1. BASK Modulation

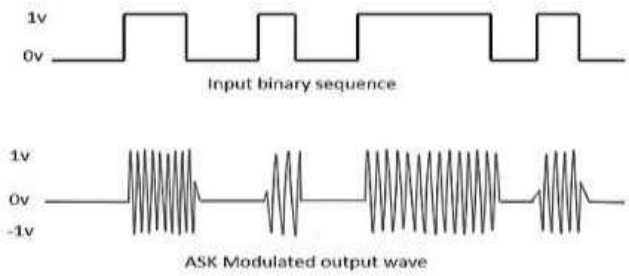


Figure 2. BASK Waveform

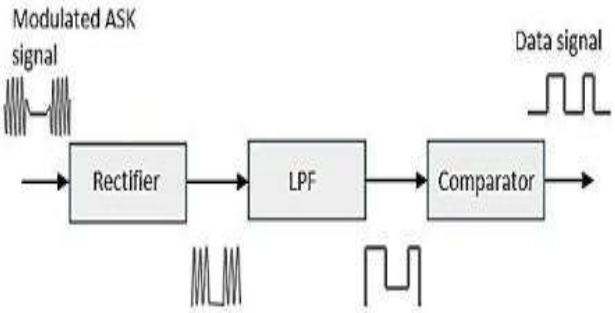


Figure 3 BASK Demodulation

In a BFSK (binary frequency-shift keying) modulation process shown in figure.4, the frequency of the sinusoidal carrier signal is changed according to the information level ("0" or "1") while keeping the amplitude and phase constant[3,4] as shown in figure 5.. The block diagram of Synchronous FSK detector[4] in figure 6 consists of two mixers with local oscillator circuits, two band pass filters and a decision circuit.

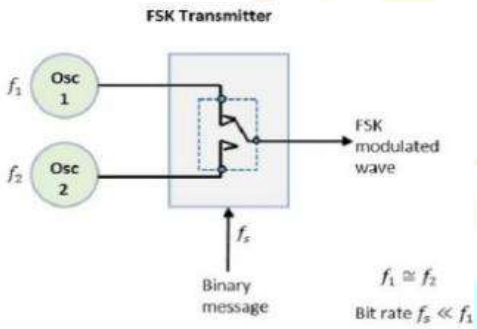


Figure 4. BFSK Modulation

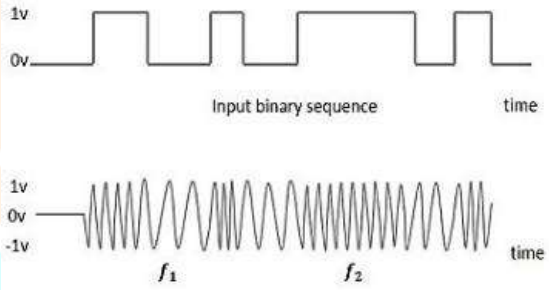


Figure 5. BFSK Waveform

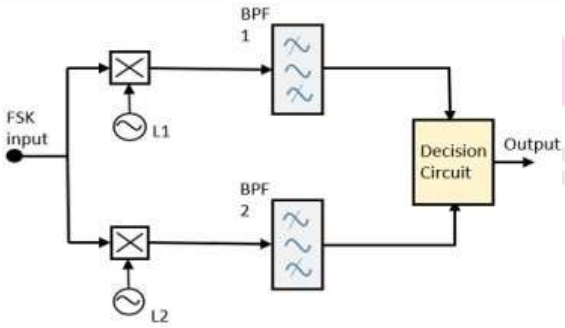


Figure 6. BFSK Demodulation

In a BPSK (binary phase-shift keying) modulation process as shown in figure.7, the phase of the sinusoidal carrier signal is changed according to the information level ("0" or "1") while maintaining the amplitude and frequency of carrier signal constant. The BPSK modulated signal is of positive values, if transmitting symbol is 1. But if transmitting signal is 0, starting of BPSK modulated signal is of negative values [3,6], 180° as shown in figure 8. This is also called as 2-phase PSK or Phase Reversal Keying. In this technique, the sine wave carrier takes two phase reversals such as 0° and 180° as shown in figure 8. Figure 9 depicts demodulation process of BPSK[3,6]

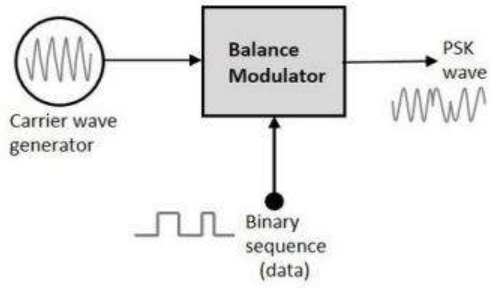


Figure 7. BPSK Modulation

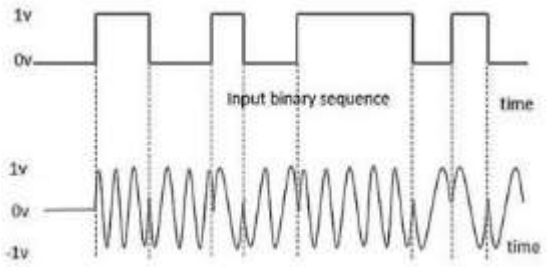


Figure 8. BPSK Waveform

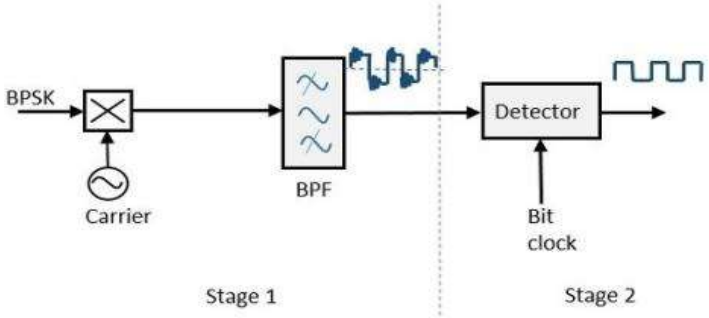


Figure 9. BPSK Demodulation

The Quadrature Phase Shift Keying (QPSK) is a variation of BPSK, and it is also a Double Side Band Suppressed Carrier (DSBSC) modulation scheme, which sends two bits of digital information at a time, called as bits. Instead of the conversion of digital bits into a series of digital stream, it converts them into bit pairs. This decreases the data bit rate to half, which allows

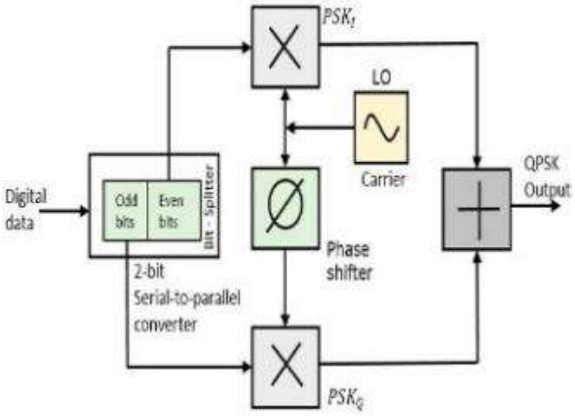


Figure 10.QPSK Modulation

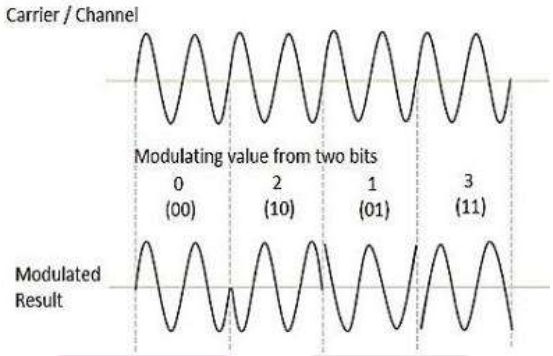
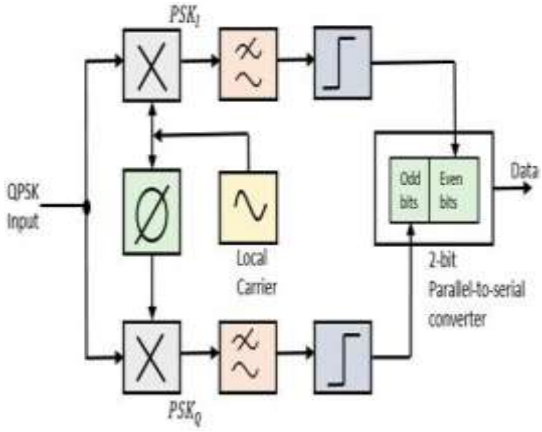
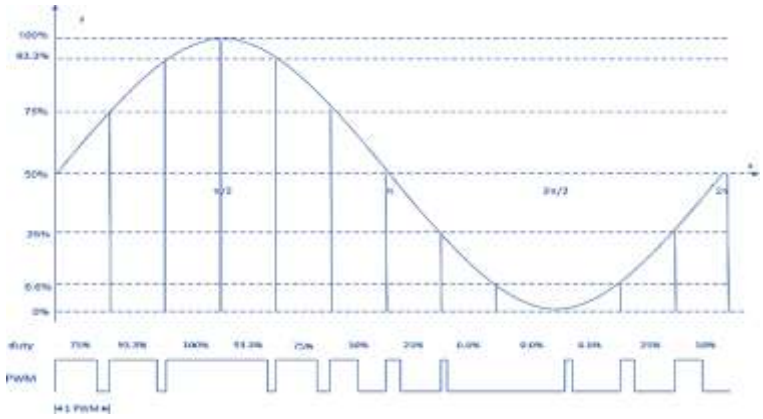


Figure 11.QPSK Demodulation

space for other users. The QPSK Modulator uses a bit-splitter, two multipliers with local oscillator, a 2-bit serial to parallel converter, and a summer circuit. At the modulator's input, the message signal's even bits (i.e., 2nd bit, 4th bit, 6th bit, etc.) and odd bits (i.e., 1st bit, 3rd bit, 5th bit, etc.) are separated by the bits splitter and are multiplied with the same carrier to generate odd BPSK (called as PSKI) and even BPSK (called as PSKQ) as depicted in figure 10. The QPSK signal is anyhow phase shifted by 90° before being modulated [5]. Figure 11 shows four different types of phase shifting for each bit pairs(00,01,10,11).

The QPSK Demodulator shown in figure 12, uses two product demodulator circuits with local oscillator, two band pass filters, two integrator circuits, and a 2-bit parallel to serial convertee[3,6].





. Figure 12.QPSK Demodulation Figure 13. Sample Point Sine Wave with The Corresponding Modulated PWM[2]

III IMPLEMENTATION

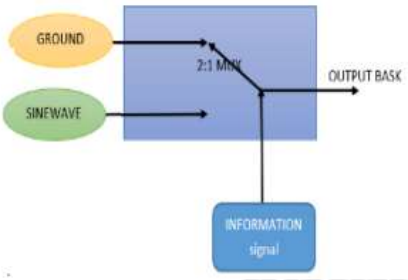
The BASK, BFSK, BPSK and QPSK Modulation and Demodulation process have been implement on programmable hardware, Altera DE1 FPGA board using Verilog HDL coding.

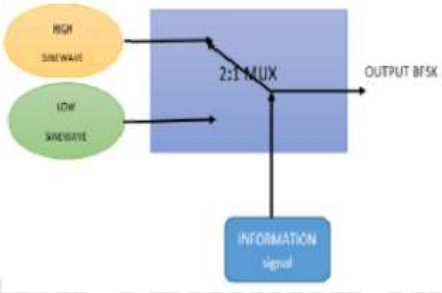
3.1 Carrier Generation

Carrier signal has been generated by Pulse Width Modulation(PWM) technique in which the inbuilt clock oscillator of 24/27/50 MHz is used. This PWM wave is passed through Low Pass Filter(LPF) to generate Sine/Cos wave. Sine wave has an ability to continuously generating a time-varying PWM. Time-varying PWM means that the duty cycle will change from one sample point to another [10] as shown in figure 13. The duty cycle at each sample point is a representation of the sine amplitude. This Pulse Width Modulation (PWM) is a method of encoding a voltage onto a fixed frequency carrier wave. Hence Verilog code of PWM technique has been written and loaded on FPGA Board. This PWM technique generates good quality (distortion free) sinusoidal waveform with minimum quantization error.

3.2 Modulation Process

Modulation process has been implemented by 2×1 multiplexer(MUX), in which binary message signal is applied as a selection line. For BASK modulation process, when binary information signal is '1', carrier will be transmitted and when it is '0', zero will be transmitted. So upper input line in 2×1 MUX will be connected to ground and lower input line with carrier signal(sine wave) as shown in figure 14. Similarly, in FSK, upper input line will be connected with carrier signal of frequency f_1 and lower will be connected with carrier signal of frequency f_2(figure 15). To generate two different frequency carrier, two different available clock frequencies are used from available three clock signals. The one of the carrier signal is phase shifted by 180° and applied as an second input in MUX to achieve BPSK modulated signal as shown in figure 16. QPSK is the two stage BPSK process in which four different phase shifted signals-0°, 90°, 180° and 270° are applied at four inputs of first stage BPSK and output will be corresponding to the input bits combination of 00, 01, 10 and 11. Table 2 shows listing of these signals at inputs of 2×1 MUX for generating BASK, BFSK, BPSK and QPSK modulated signal.





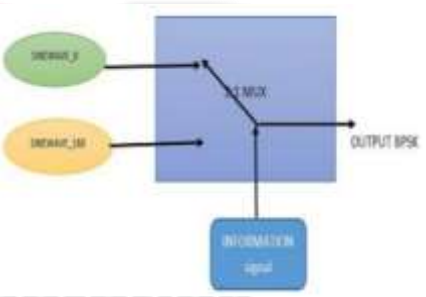


Figure 14. BASK Realization Figure 15. BFSK Realization Figure 16. BPSK Realization

3.3 Demodulation Process

In demodulation process as depicted in figure 17, incoming modulated signal is multiplied with carrier and then added with all the samples, multiplied, from a period. This operation takes place in the accumulator. Once we have a result, it is compared with a threshold. If the compared signal is positive, the demodulator takes the decision that '1' was transmitted, otherwise, '0'[4,6].

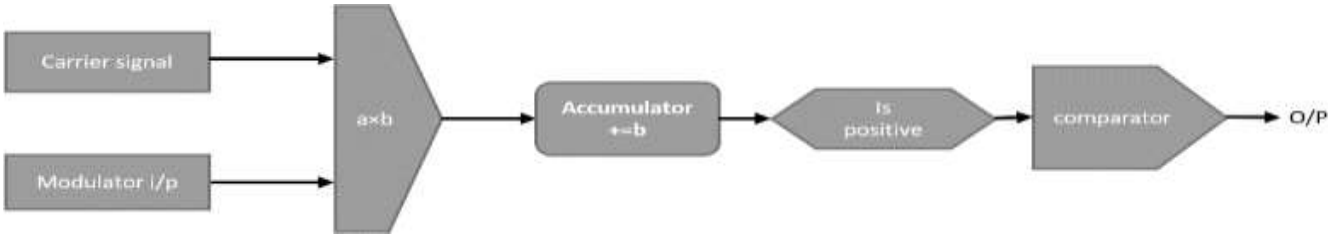


Figure 17 Demodulation Process

Table 1: Modulation Process- 2×1 MUX Input Signals

Modulation Techniques	Multiplexer input signal 1	Multiplexer input signal 2
BASK	Carrier Signal	Ground
BFSK	Carrier Signal with frequency f_1	Carrier Signal with frequency f_2
BPSK	Carrier Signal with 0° phaseshift	Carrier Signal with 180° phase shift
QPSK	$BPSK_1$	$BPSK_2$

IV RESULTS AND DISCUSSION

For implementation of Modem(**MO**dulation-**DEM**odulation) on DE1 FPGA board, certain steps are required to be followed. The simulation of Verilog code and pin assignment have been taken place in Quartus-II Altera simulator. To load program on board, bit file known as. SOF (SRAM Object File) is generated for each Modem through 'Programmer'. Figure 18 shows implementation flow starting from PC to DSO. The signal has been fetched from FPGA board and apply to externally implemented LPF on bread board to extract carrier signal. This carrier signal applied to FPGA board for modulation and demodulation process, and generated signals are observed on DSO. Since DSO has only two channels, signals are observed step by steps. Figure 19 depicts two FPGA board, LPF on bread board and dual channel Digital Storage Oscilloscope(DSO).

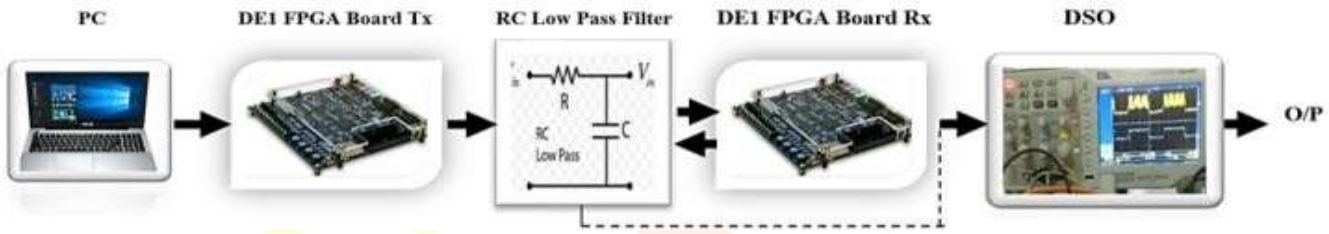


Figure 18. Implementation Flow

The voltage and frequency of carrier signals generated for modulation and demodulation process have been listed in Table 2. The different clock frequency is used from FPGA board to generate PWM signal for each individual techniques. As per the PWM algorithm [2], generated PWM signal frequency and sine wave(carrier) signal frequency has been calculated for sample value of 256 and Clock frequency of 27 MHz as follow.

Table 2: Amplitude and Frequency of Signals

Signal	BASK	BFSK	BPSK	QPSK
Input Voltage	5V	5V	5V	5V
Input Clock Freq in MHz(on FPGA board)	27	27, 50	27	27, 50
PWM Freq - in KHz	105	105, 195	105	105, 93
Carrier signal frequency .in Hz	411	411, 811	411	411, 811
Carrier Signal Amplitude	1.5V	1.6V, 2V	1.5V	1.6V, 2V

- **CLK frequency = 27MHz**
- **Sample value = 256**

$$T_{CLK} = \frac{1}{Fclk} = \frac{1}{27MHZ} = 3.7ns$$

$$= 3.7ns \times 256 = 9.4us$$

$$Fpwm = \frac{1}{Tclk} = 1\backslash 9.4ns = 105\ KHz$$

$$Fsine = \frac{Fpwm}{sample} = \frac{105KHz}{256} = 411\ Hz$$

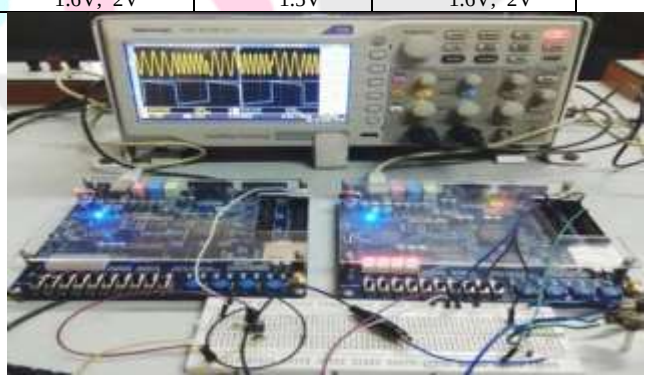


Figure 19 Experiment Setup

Figure 20 shows PWM signal(top) obtained through verilog coding to generate sine wave(bottom) which is use as a carrier signal. The carrier signal of 414Hz is the output after LPF. Figure 21, 22 and 23 shows BASK, BFSK and BPSK modulated signals. Since QPSK is generated by combining two BPSK block, and PSK_I will be same as figure 23 and other two phase shifted signals are obtained by second MUX for PSK_Q Signal(not shown) Fig. 24 shows demodulation of BASK. When signal is present, output is logic '1' and when signal is absent output is logic '0'. Fig. 25 shows demodulation of BFSK signal, in which it is observed that for low frequency signal, output is logic '1' and for high frequency, output is logic '0'. BPSK Demodulated signal is shown in figure 26. Ripple is present due to imperfect filtering and this signal is applied to comparator with proper threshold voltage to generate perfect binary information signal. Figure 27 shows extracted information signal and transmitted information signal.

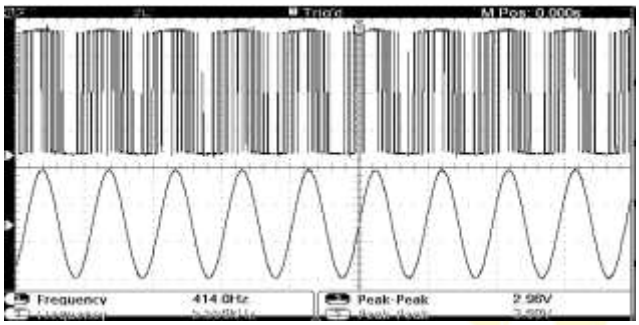


Figure 20 Carrier Generation

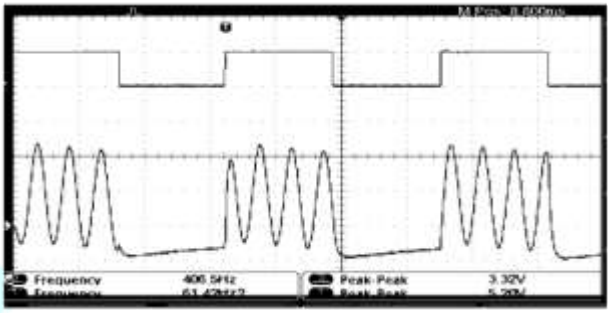


Figure 21 ASK Modulation

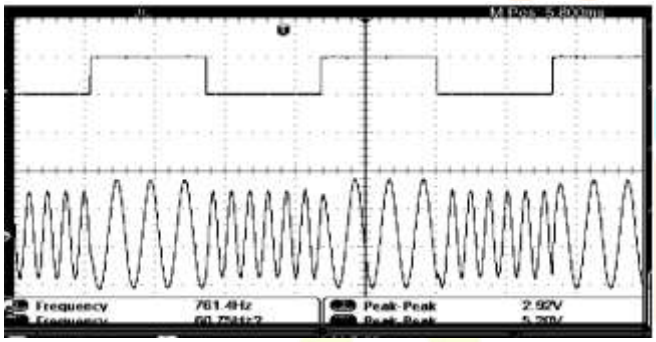


Figure 22 FSK Modulation

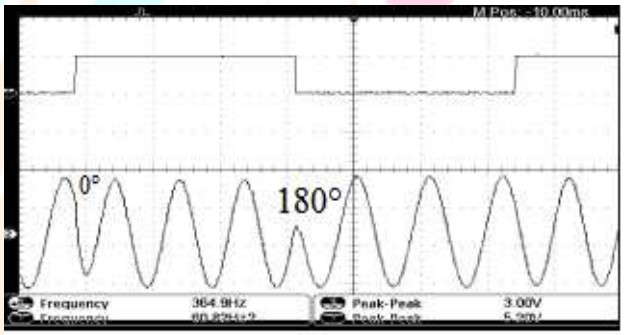


Figure 23 PSK Modulation

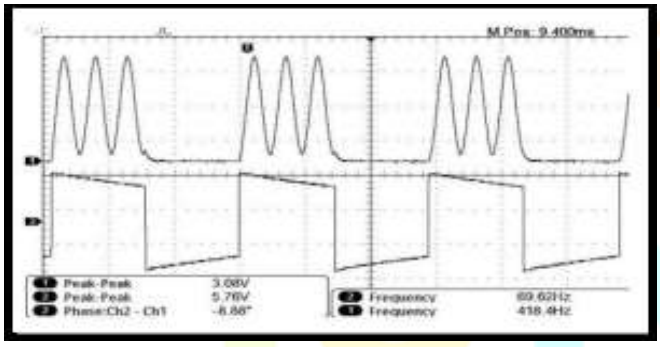


Figure 24 ASK Demodulation

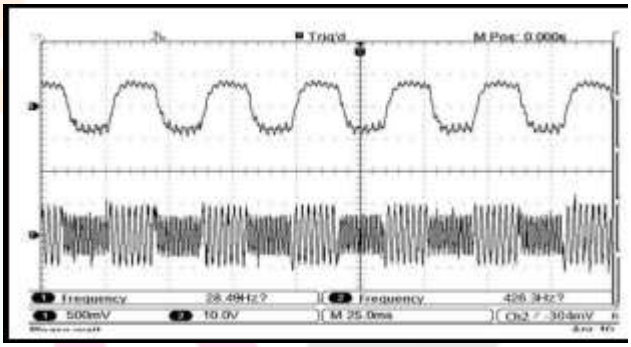


Figure 25 FSK Demodulation

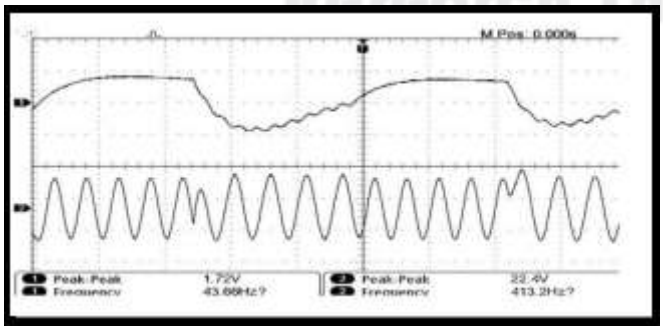


Figure 26 PSK Demodulation

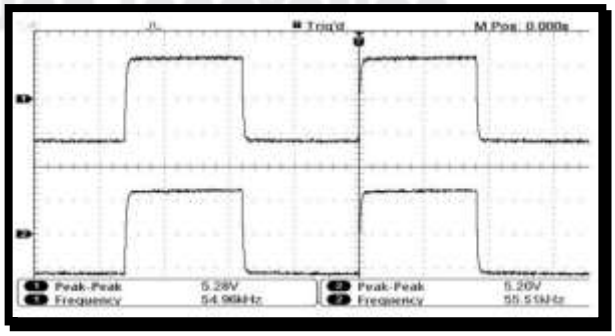


Figure 27 Transmitted and Received Information Signal

Digital Modulation and demodulation techniques have been implemented on different FPGA kit and Table 3 shows comparison of hardware utilization within a chip for these different techniques. The number of Look up Table(LUT)s are required more in BFSK, BPSK and QPSK compare to BASK because in BASK, one single sine wave signal is required while in BFSK and BPSK two sine wave signal and in QPSK four sine wave singlesare required to do modulation of message signal. Percentage utilization shows the amount of hardware used on FPGA board from available inbuilt resources. QPSK technique requires highest memory bits for storing four different phase shifted sine wave.

Table 3: Device Utilization for Digital Modulation and Demodulation Process on DE-1 FPGA Board

FPGA	BASK	BFSK	BPSK	QPSK
No. of Clock	1	2	1	2
LUTs* for Modulation	186	369	369	398
LUTs* for Demodulation	201	234	276	349
Total Memory Bit	239.67	239.69	239.67	439.69
Utilization-for Modulation	1%	2%	2%	4%
Utililzation- for Demodulation	1%	1%	2%	3%

*LUT=Look up Table

IV CONCLUSION

Four Modem BASK, BFSK, BPSK and QPSK have been successfully implemented on Altera DE1 FPGA board of Spartan family. Programs for each building block for modulation & demodulation systems were written in Verilog HDL. The implemented modem techniques require minimum number of hardware utilization like LUTs, registers and memory bit. Hence, it is possible to implement all such types of modulation and demodulation techniques on a single FPGA chip and can be utilized in communication system with minimum hardware. Minimization of hardware not only provides small size but also reduces power consumption as well as improves speed of the system with added features of FPGA reconfigurability.

FUTURE SCOPE

Channel noise can be added with modulated signal to check performance of demodulation process real time. This implementation can be extended further from QPSK to 8PSK. Advanced modulation techniques can be implemented like 16 QAM, MSK, GMSK.

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