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Multi Threshold CMOS Technique for designing of Low Power 4 Bit ALU and Combinational Circuits

Prachi, Prof KL Purshnani
M.Tech Student, HOD
Department of Electronics and Communication Engineering
Babu Banarsi Das Institute of Technology, Ghaziabad, Uttar Pradesh, India

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ABSTRACT: Exponential increase in the transistor density on a single substrate in an integrated circuit has paved the way for tremendous growth in the semiconductor industry. Very Large Scale Integration (VLSI) of these transistors on a single substrate boosts performance but also causes multiple issues related to delay and power consumption. It is important to boost performance but keep the trade-offs related to delay and power to a minimum. This has resulted in researchers moving towards low-power design techniques. Such techniques are different from conventional design techniques in such a way that power is consumed as and when needed. This helps in minimizing the total power consumed by any circuit. The work presented in this paper aims to present the capability of the multiple threshold complementary metal oxide semiconductor (MTCMOS) technique to achieve low power consumption with approximately the same delay time in a single circuit. Standard arithmetic and logic circuits have been simulated at the 180 nm technology node and critical parameters, namely power, and delay have been calculated using the MTCMOS technique and compared with conventional CMOS design. It is shown that power consumption is significantly reduced by using transistors of different thresholds (as in the MTCMOS technique).

1. INTRODUCTION

In today's technology, low-power, and high-speed systems are highly preferable. Circuit Designers need to comprehend how low-power methods influence performance characteristics and need to choose a lot of strategies that are predictable with these properties [3].In current CMOS advances, subthreshold leakage current is bigger than other leakage current segments. As technology scales reduce, the reduction of the threshold voltage (Vth) and supply voltage (VDD) causes an exponential increase in sub-threshold leakage power, Sub-threshold leakage is the current flowing between the source and drain during weak inversion mode when the transistor is in turn off state. Limiting leakage power is a significant undertaking in convenient devices to build battery life.Fig.1 (IJEST, JULY 2014) shows static
power is comparable to dynamic power with the current trend of technology scaling. Numerous strategies have been proposed to diminish leakage power. Multi-threshold CMOS (MTCMOS) technique reduces low-power power during standby mode which is an effective circuit-level technique[2]. MTCMOS logic provides low-power and high-speed designs with no area overhead. In the CMOS logic circuits, power dissipation is an important factor. In the present technology, threshold Voltages & supply voltages for MOS transistors are decreased.

Leakage current is the current that flows from drain to source when it is in the off state which depends on oxide thickness, gate length that varies exponentially with temperature, threshold voltage, and many other parameters.

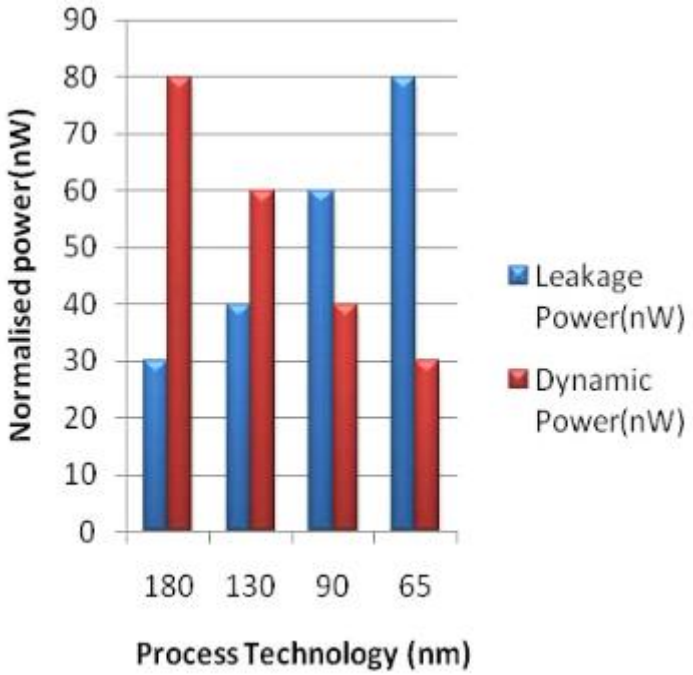

Fig. 1 Leakage and dynamic power consumption with technology scaling (IJEST, JULY 2014)

1.1 MTCMOS Technique

Low-power design strategies extend from the device/process level to the algorithmic dimension. Subthreshold leakage power is characterized by a little increase by scaling both the supply voltage and the threshold voltage, whereas dynamic power is decreasing quadratically under modern CMOS advancements. To make up for the presentation misfortune because of a lower supply voltage, a transistor's threshold voltage (VT) ought to likewise be decreased. Because of this, there is an exponential increment in the subthreshold leakage current. In this manner, To lessen the subthreshold leakage current brought about by the diminished VT technique is a significant research region today.

Multi-threshold is one kind of CMOS which is a deviation in the chip technology. It has a transistor with multiple threshold voltages to optimize delay or power[2]. It can accomplish a lower threshold voltage, and in this way, then the higher performance is just a little standby leakage current. The basic threshold of making MOS with various threshold voltages is to apply various bias voltages to the body or substrate terminal of the transistors. It empowers superior performance and low power activity, however requires consecutive circuit structures that can hold during standby modes. However, In this technique, the transistor is isolated from the power supply in standby mode. As a result, the circuit becomes fast in active mode. The mode degrades due to the presence of sleep transistors. Thusly, the sleep transistor measuring is basic as oversizing prompts area penalty and under sizing prompts performance degradation and diminished noise margin.

A decrease in power dissipation is a standout amongst the most significant issues in VLSI design today. An enormous part of total power dissipation is because scaling is brought about
by subthreshold leakage currents[1]. The Multi-Threshold CMOS (MTCMOS) is an alluring system to lessen subthreshold leakage currents during standby modes by using high-Vth control switches (sleep transistors). For the compelling leakage power decrease, the Sleep transistor gives diverse VT. Low VT has fast yet in addition to high power utilization, High VT has low power consumption yet low speed as well.

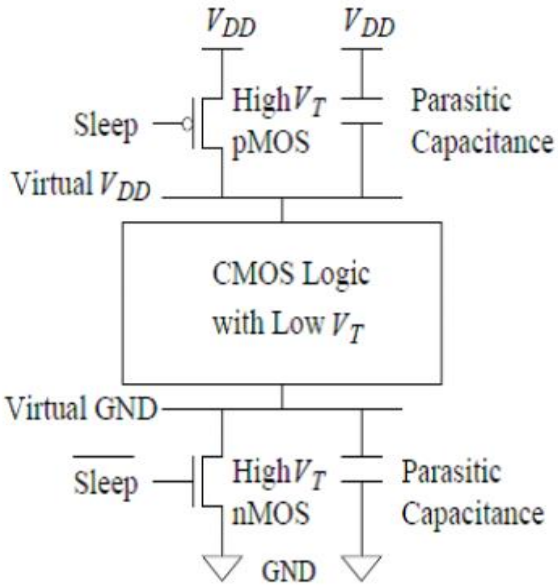

Fig 2. Generic structure of MTCMOS logic gate (IJEST, JULY 2014)

Low VT is utilized to diminish the propagation delay time in the critical path, and High VT is utilized to decrease the power utilization in the shortest path. The circuit is designed with sleep and active operation mode[4]. This paper describes a high-speed and low-power design for basic gates, and full adder circuits with MTCMOS technology.

2. CIRCUIT DESIGN OF NAND GATE

A The pull-up and pull-down networks are the main components of conventional CMOS circuits. There is a difference between a pull-up network and a pull-down network, which consists of PMOS transistors and NMOS transistors, respectively. In this technique, all PMOS transistors must have either an input from another PMOS transistor or from the power supply voltage (VDD)[3]. Similarly, all NMOS transistors must have either an input from another NMOS transistor or from the ground. Fig. 2.1 (Kang et al. 2003) shows the circuit diagram of a two-input NAND gate using this technique. 2-input NAND gate is a universal gate, in which both PMOS are in parallel whose source is connected to VDD. While the NMOS are in series and connected to GND.

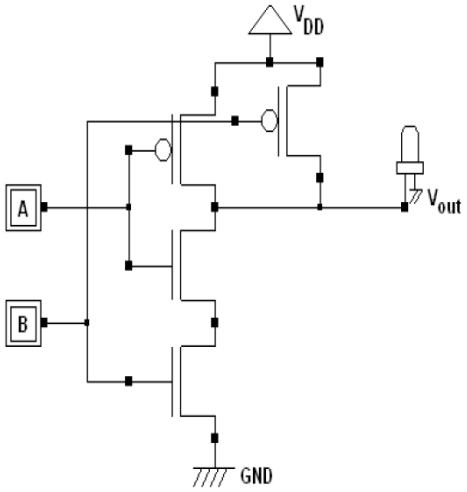

Fig2.1 2 input NAND gate using conventional CMOS (Kang et al. 2003)

2.1 BY MTCMOS TECHNIQUE

In MTCMOS technique, a high-V_T PMOS transistor (sleep PMOS transistor) is placed between the power supply voltage (VDD) and the logic circuit; and a high-V_T NMOS transistor (sleep NMOS transistor) is inserted between the ground and logic circuit. Fig. 2.2 shows the circuit diagram of a two-input NAND gate

using this technique[1]. During the active mode of operation, the high threshold voltage MOS transistors (sleep transistors) are turned on, While during sleep mode, these high VTH transistors are turned off.

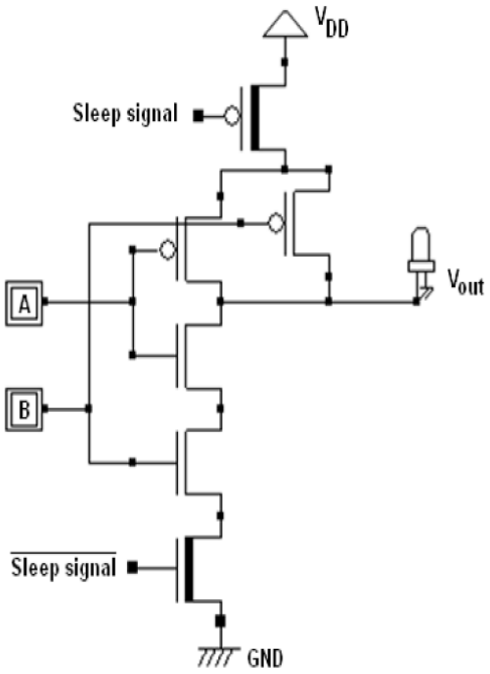

Fig2.2 2 input NAND gate by MTCMOS technique (Mutoh et al. 1995)

3. CIRCUIT DESIGN OF FULL ADDER

Logic circuits that add numbers are called full adders. With the full adder, two bits can be added along with a third bit, which is called carrying [2]. Figure 2.3 illustrates a conventional one-bit full adder. The MTCMOS technique is used to implement full adder logic in this paper. A comparison of the static and average powers of the above techniques, as well as conventional circuits, is made. Adder logic performs addition during active mode when sleep
transistors are ON. In standby mode, the high Vth sleep transistors of the adder are turned off to cut off the circuit from the supply rails. Suppose we have three bits A, B, and Cin (input carry) that are input to the XOR gate, then the Boolean function for the full adder can be given as.

Sum = A (EXOR) B

Carry = AB + (A (EXOR) B) Cin

Fig. 2.3 shows 1-bit full adder logic diagram. The full adder contains 3 inputs (A, B, Cin) and 2 outputs (Sum and Carry).

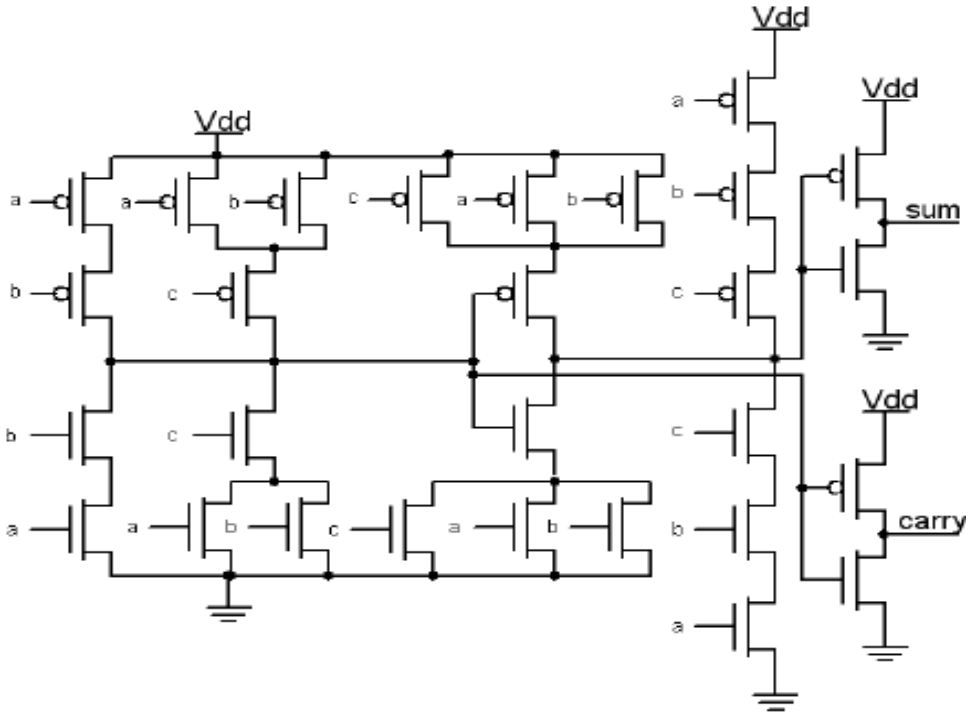

Fig 2.3 Conventional Circuit of FULL ADDER

3.1 CIRCUIT DESIGN USING MTCMOS TECHNIQUE

MTCMOS (Multi-Threshold Complementary Metal Oxide Semiconductor) technique has risen as a mainstream and promising circuit technique for performance improvement (for example power minimization and decrease in delay) of full adder. In this MTCMOS technique, a high Vt sleep transistor is included as a footer (NMOS) or header (PMOS) to the circuit. The schematic of a proposed MTCMOS adder circuit with N-Type sleep transistor associated as footer between ground rail and logic circuit. The logic gate ground rails are connected to the virtual ground network; which has a slightly high potential compared to real ground. And then, the virtual and real ground networks are linked by the sleep transistor[1]. The schematic of the MTCMOS full adder is shown in Fig. 2.4

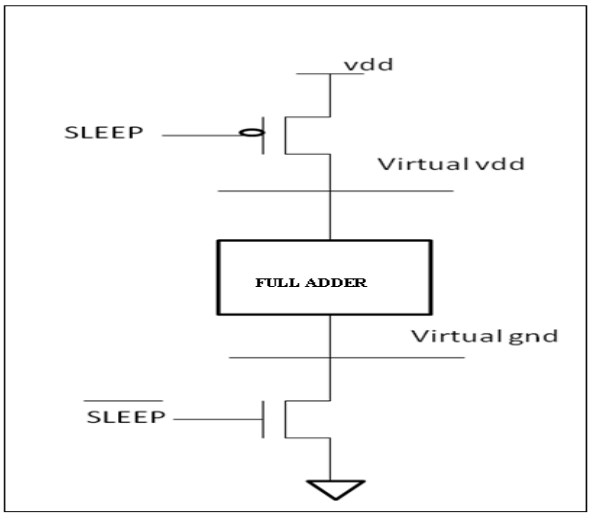

Fig 2.4 MTCMOS Circuit of Full Adder

4. 4-Bit ALU Circuit

Arithmetic and the logical unit is the critical component of the microprocessor. It is the core component of the CPU. ALU consists of logic gates like AND, OR gate, ADDER, SUBTRACTOR, and MUX. The 4-Bit ALU was formed by combining 4 1-bit ALU as shown in Fig 2.5. It consists of 5 multiplexers. A single 4-bit ALU is having the same design as that of the circuit of the 74S181 of Texas Instruments. The idea behind using this IC was that it performs a large number of arithmetic and logical operations. As ALU is one of the

most power-consuming components. So for reducing its power all of its components' power consumption should be reduced. For that, we are optimizing the power and delay of each component using the MTCMOS technique[4].

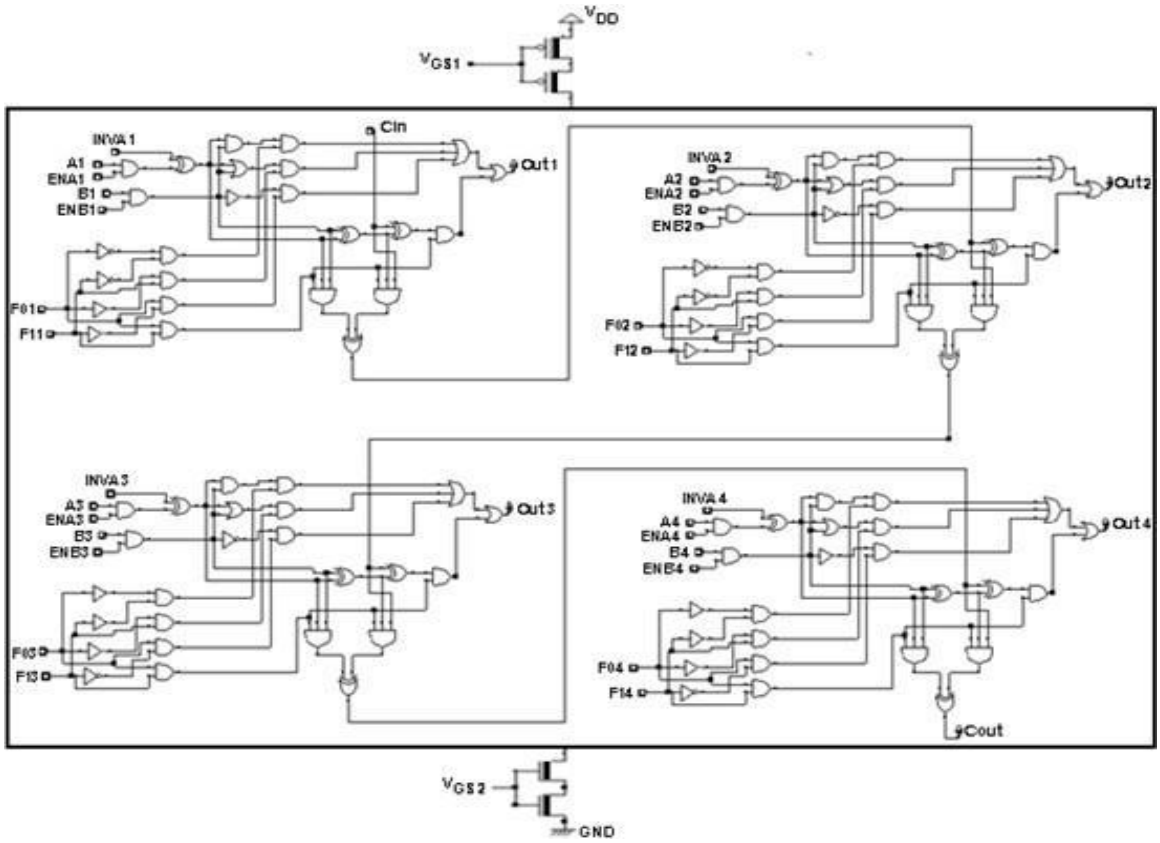

Fig 2.5 MTCMOS 4-Bit ALU

5. RESULT

The proposed universal gates, full adder, and multiplier circuits are simulated using a cadence virtuoso tool with 180nm process technology.

CIRCUIT	TECHNIQUE	STATIC POWER (W)	DELAY (SEC)
NAND	CMOS	376 x 10^{-12}	200 x10^{-12}
	MTCMOS	2.34 x 10^{-12}	300 x 10^{-12}
FULL ADDER	CMOS	2.359 x 10^{-12}	22.71 x 10^{-12}
	MTCMOS	2.884 x 10^{-12}	30.13 x 10^{-12}

5.1 4-Bit ALU (Arithmetic Logic Unit)

5.1.1 POWER (W)

OPERATION	ALU(CMOS)	ALU(MTCMOS)	INPUT
ADDITION	27.5×10^{-12}	21.5×10^{-12}	a = 0, b = 0
SUBTRACTION	24.53×10^{-12}	18.14×10^{-12}	a = 1, b = 0
OR	26.04×10^{-12}	15.96×10^{-12}	a = 0, b = 1
AND	23.05×10^{-12}	16.5×10^{-12}	a = 1, b = 1

5.1.2 DELAY (sec)

OPERATION	ALU(CMOS)	ALU(MTCMOS)	INPUT
ADDITION	37.59×10^{-12}	42.5×10^{-12}	a = 0, b = 0
SUBTRACTION	23.47×10^{-12}	25.40×10^{-12}	a = 1, b = 0
OR	30.69×10^{-12}	33.23×10^{-12}	a = 0, b = 1
AND	35.32×10^{-12}	40.61×10^{-12}	a = 1, b = 1

CONCLUSION

CMOS logic with multiple thresholds is presented in this paper as an effective standby leakage control method. MOS transistors with low thresholds and high thresholds can greatly reduce leakage power using MTCMOS. Based on the simulation results, we can conclude that MTCMOS is capable of achieving a reduction in power and delay over conventional methods.

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