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DESIGN AND IMPLEMENTATION OF MULTILEVEL INVERTERS FOR ELECTRIC VEHICLES

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ABSTRACT:

The efficient and compact design of multilevel inverters (MLI) motivates in various applications such as solar PV and electric vehicles (EV). This paper proposes a 17-Level multilevel inverter topology based on a switched capacitor (SC) approach. The number of levels of MLI is designed based on the cascade connection of the number of SC cells. The SC cells are cascaded for implementing 53 and 33 levels of the output voltage. The proposed structure is straightforward and easy to implement for the higher levels. As the number of active switches is less, the driver circuits are reduced. This reduces the device count, cost, and size of the MLI. The solar panels, along with a perturb and observe (P&O) algorithm, provide a stable DC voltage and is boosted over the DC link voltage using a single input and multi-output converter (SIMO). The proposed inverters are tested experimentally under dynamic load variations with sudden load disturbances. This represents an electric vehicle moving on various road conditions. A detailed comparison is made in terms of switches count, gate driver boards, sources count, the number of diodes and capacitor count, and component count factor. For the 17-level, 33-level, and 53-level MLI, simulation results are verified with experimental results, and total harmonic distortion (THD) is observed to be the same and is lower than 5% which is under IEEE standards. A hardware prototype is implemented in the laboratory and verified experimentally under dynamic load variations, whereas the simulations are done in MATLAB/Simulink.

Keywords **-** Multilevel inverter, photovoltaic (PV) system, maximum power point tracking (MPPT), electric vehicles (EV), total harmonic distortion (THD).

I INTRODUCTION

Recently, because of increasing oil prices and environmental concerns, hybrid electric vehicles (HEVs) are gaining increased attention due to their higher efficiencies and lower emissions associated with the development of improved power electronics and motor technologies. An HEV typically combines a smaller internal combustion engine of a conventional vehicle with a battery pack and an electric motor to drive the vehicle. The combination offers lower emissions but with the power range and convenient fueling of conventional (gasoline and diesel) vehicles. Though the HEVs have a backup combustion engine, the batteries need to be charged regularly.HEVs need a traction motor and a power inverter to drive the traction motor. The requirements for the power inverter include high peak power and low continuous power rating. Currently available power inverter systems for HEVs use a dc–dc boost converter to boost the battery voltage for a traditional three-phase inverter. If the motor is running in a high power mode, the dc–dc boost converter will boost the battery voltage to a higher voltage, so that the inverter can provide higher power to the motor. Present HEV traction drive inverters have low power density, are expensive, and have low efficiency because they need bulky inductors for the dc–dc boost converters. Multilevel inverter can increase the power by (m-1) times than that of two level inverter through the series and parallel connection of power semiconductor switches. Comparing this with two level inverter systems delivering same power, multilevel inverter has the advantages that the lower harmonic components on the output voltages can be eliminated and EMI problem could be decreased. Due to these merits, many studies on multilevel inverters have been performed at simulations and very few with the hardware implementations.

CHAPTER-2

NONCONVENTIONAL ENERGY SOURCES

2.1 INTRODUCTION

In this chapter, the nonconventional energy sources in the project are discussed briefly just likes Wind system, Hydro system, PV system, & Battery's etc... With necessary definitions and basic information about them.

2.2 Schematic diagram of the proposed multi-input inverter

2.3 SOLAR PHOTOVOLTAICS

2.3.1 Introduction

The conversion of solar radiation occurs by the photovoltaic effect which was first observed by Becquerel. It is quite generally defined as the emergence of an electric voltage between two electrodes attached to a solid or liquid system upon shining light onto this system. Energy conversion devices which are used to convert sunlight to electricity by the use of the photo-voltaic effect are called solar cells. Single converter cell is called a solar cell or more generally photovoltaic cell and combination of such cells designed to increase the electric power output is called a solar module or solar array and hence the name 'Photovoltaic Arrays'. Solar cells can be arranged into large groupings called arrays. These arrays, composed of many thousands of individual cells, can function as central electric power stations, converting sunlight into electrical energy for distribution to industrial, commercial and residential users. Solar cells in much smaller configurations are commonly referred to as solar cell panels or simply panels. Practically, all photovoltaic devices incorporate a P-N junction in a semiconductor across which the photo voltage is developed. The solar panels consist mainly of semiconductor material, with Silicon being most commonly used.

2.3.2 Basics of Solar Cells

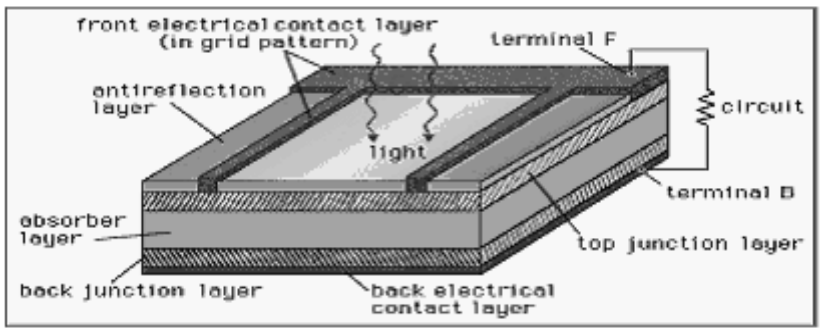


Fig.2.2: Solar cell

The overwhelming majority of solar cells are fabricated from silicon with increasing efficiency and lowering cost as the materials range from amorphous (non-crystalline) to polycrystalline to crystalline (single crystal) silicon forms. Unlike batteries or fuel cells, solar cells do not utilize chemical reactions or require fuel to produce electric power and unlike electric generators, they do not have any moving parts.

Light enters the device through an optical coating, or antireflection layer that minimizes the loss of light by reflection; it effectively traps the light falling on the solar cell by promoting its transmission to the energy-conversion layers below. The antireflection layer is typically an oxide of silicon, tantalum or titanium that is formed on the cell surface by spin coating or a vacuum deposition technique.

The three energy-conversion layers below the antireflection layer are the top junction layer, the absorber layer, which constitutes the core of the device, and the back junction layer. Two additional electrical contact layers are needed to carry the electric current out to an external load and back into the cell, thus completing an electric circuit. The electrical contact layer on the face of the cell where light enters is generally present in some grid pattern and is composed of a good conductor such as a metal. Since metal blocks light, the grid lines are as thin and widely spaced as is possible without impairing collection of the current produced by the cell. The back electrical contact layer has no such diametrically opposed restrictions. It needs to simply function as an electrical contact and thus cover the entire back surface of the cell structure. Because the back layer also must be a very good electrical conductor, it is always made of metal. Since most of the energy in sunlight and artificial light is in the visible range of electromagnetic radiation, a solar cell absorber should be efficient in absorbing radiation at those wavelengths. Materials that strongly absorb visible radiation belong to a class of substances known as semiconductors. Semiconductors in thicknesses of about one-hundredth of a centimeter or less can absorb all incidents visible light; since the junction-forming and contact layers are much thinner, the thickness of a solar cell is essentially that of the absorber. Examples of semiconductor materials employed in solar cells include Silicon, Gallium Arsenide, Indium Phosphide and Copper Indium Selenide.

When light falls on a solar cell, electrons in the absorber layer are excited from a lower-energy "ground state," in which they are bound to specific atoms in the solid, to a higher "excited state" in which they can move through the solid. In the absence of the junction-forming layers, these "free" electrons are in random motion and so there can be no oriented direct current. The addition of junction-forming layers, however, induces a built-in electric field that produces the photovoltaic effect. In effect, the electric field gives a collective motion to the electrons that flow past the electrical contact layers into an external circuit where they can do useful work.

There are several approaches to manufacturing solar cells, including the kind of semiconductor used and the crystal structure employed, with each different factor affecting the efficiency and cost of the cell. Other external factors such as the ambient weather conditions like temperature, illumination, shading, etc., also affect the solar panel's output. The aim is to design a system that will extract the most possible power regardless of ambient weather conditions or solar cell efficiency.

2.3.3 Solar Cell Characteristics

The current-to-voltage characteristic, power-to-voltage characteristics of a solar cell are non-linear, which make it difficult to determine the maximum power point. It is straightforward to determine the maximum power point on a linear curve as maximum power is transferred at the midpoint of the current-voltage characteristic. A typical V-I characteristic of solar cell is shown in Fig 2.3.

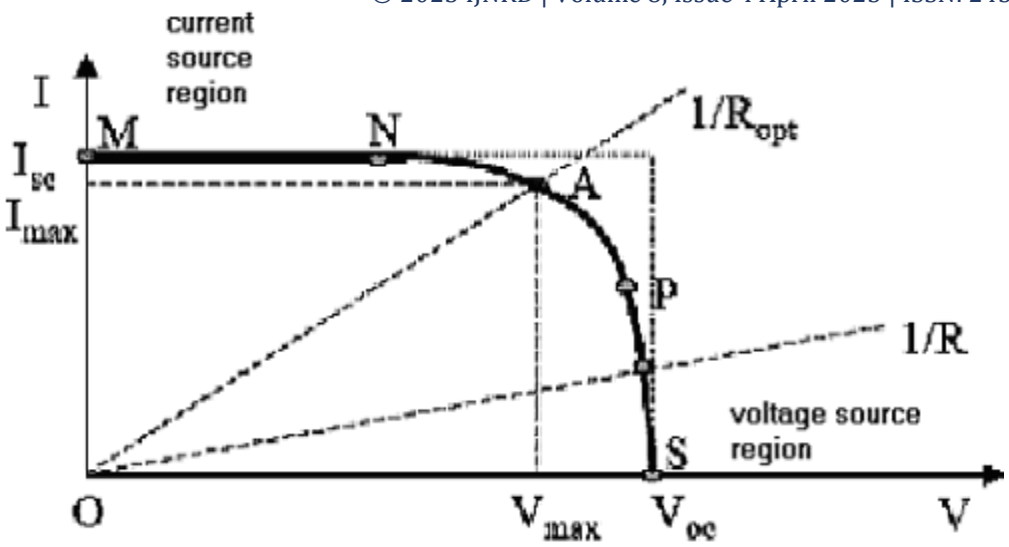


Fig.2.3 charecteristics of solar cell

For a solar cell, the non-linear relationship means the maximum power point has to be determined by calculating the product of the voltage and output current. In order to extract maximum power from the solar cell, the solar cell must always be operated at or very close to where the product of the voltage and output current is the highest. This point is referred to as the maximum power point (MPP) and it is located around the 'bend' or 'knee' of the I-V characteristic.

The operating characteristic of a solar cell consists of two regions: the current source region and the voltage source region. In the current source region, the internal impedance of the solar cell is high and this region is located on the left side of the current-voltage curve. The voltage source region, where the internal impedance is low, is located on the right side of the current-voltage curve. As can be observed from the characteristic curve, in the current source region, the output current remains almost constant as the terminal voltage changes and in the voltage source region, the terminal voltage varies only minimally over a wide range of output current.

According to the maximum power transfer theory, the power delivered to the load is maximum when the source internal impedance matches the load impedance. For the system to operate at or close to the MPP of the solar panel, the impedance seen from the input of the MPPT needs to match the internal impedance of the solar panel. Since the impedance seen by the MPPT is a function of voltage (V = I * R), the main function of the MPPT is to adjust the solar panel output voltage to a value at which the panel supplies the maximum energy to the load. However, maintaining the operating point at the maximum power point can be quite challenging as constantly changing ambient conditions such as irradiance and temperature will vary the maximum power operating point. Hence, there is a need to constantly track the power curve and keep the solar panel operating voltage at the point where the most power can be extracted.

Irradiance is a characteristic related to the amount of Sun energy reaching the ground, and under ideal conditions it is measured as 1000 W/m^2 at the equator. The sun energy on the earth is highest around the equator when the sun is directly overhead. Some important magnitudes related to irradiance include the spectral irradiance, irradiance and radiation. Spectral irradiance is the power received by a unit surface area at a particular wavelength, while

irradiance is the integral of the spectral irradiance extended to all wavelengths of interest. Radiation is the time integral of the irradiance extended over a given period of time.

In designing PV systems, the main concern is the radiation received from the sun at a particular location at a given inclination angle and orientation and for long periods of time. Since solar radiation is the energy resource of the solar panel, the output of the panel is significantly affected by changing irradiance. The I-V and P-V characteristics of a solar cell including the effects of irradiance are shown in Fig 2.4.

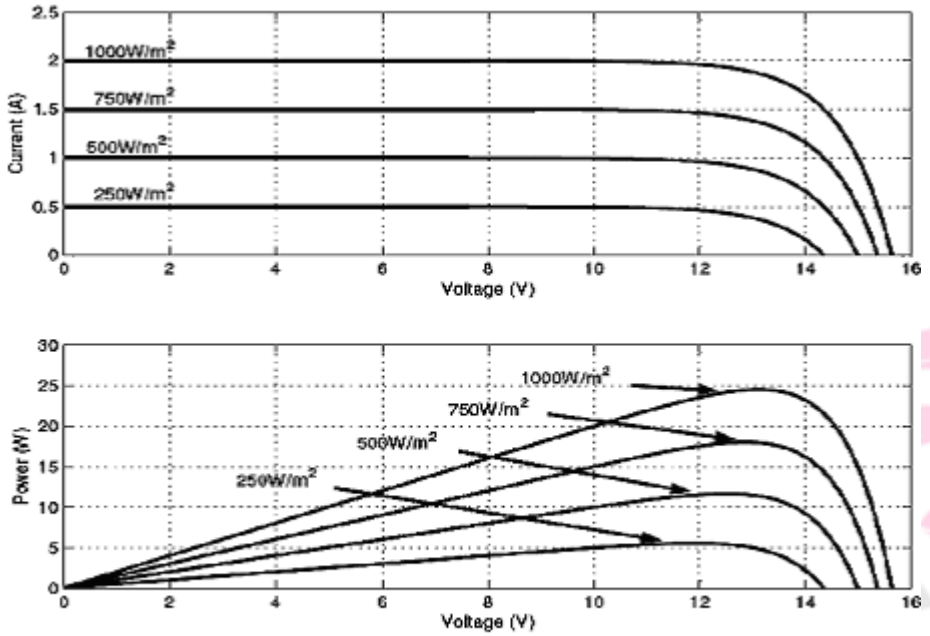


Fig.2.4:I-V and P-V Charecteristics of a solar cell for various Irradiance

The irradiance at any location is strongly dependent on the orientation and inclination angles of the solar panel. Orientation is usually measured relative to the south in northern latitudes while it is measured relative to the north in southern latitudes. On the other hand, the inclination angle is measured relative to the horizontal. Using these two parameters, the irradiation at any location can be determined. The irradiance information for many sites worldwide is widely available.

As it can be observed from Fig 2.4, the output power is directly proportional to the irradiance. As such, a smaller irradiance will result in reduced power output from the solar panel. However, it is also observed that only the output current is affected by the irradiance. This makes sense, since by the principle of operation of the solar cell the generated current is proportional to the flux of photons. When the irradiance or light intensity is low, the flux of photon is less than when the sun is bright and the light intensity is high, thus more current is generated as the light intensity increases.

The change in voltage is minimal with varying irradiance and for most practical applications, the change is considered negligible.

Although irradiance is an important factor in determining the I-V characteristic of a solar panel, it is not the only factor. Temperature also plays an important role in predicting the I-V characteristic, and the effects of both factors have to be considered when designing a PV system. Whereas the irradiance mainly affects the output current, the

temperature mainly affects the terminal voltage. A plot of I-V and P-V characteristic with varying temperature is shown in Fig 2.5.

It is observed from Fig 2.5 that the terminal voltage increases with decreasing temperature. One of the reasons the solar panel operates more efficiently with decreasing temperature is due to the electron and hole mobility of the semiconductor material. As temperature increases, the electron and hole mobility in the semiconductor material decreases significantly. The electron mobility for Silicon at 25º C is about 1700cm2/volt-sec and will decrease to about a fourth of this value as temperature increases to 225º C and likewise the hole mobility decreases from about 600cm2/volt-sec at 25ºC to 200cm2/volt-sec as temperature increases to 225ºC. While the higher reference temperatures are not realistic operating conditions for a solar panel, it does show that electron and hole mobility decrease with increasing temperature.

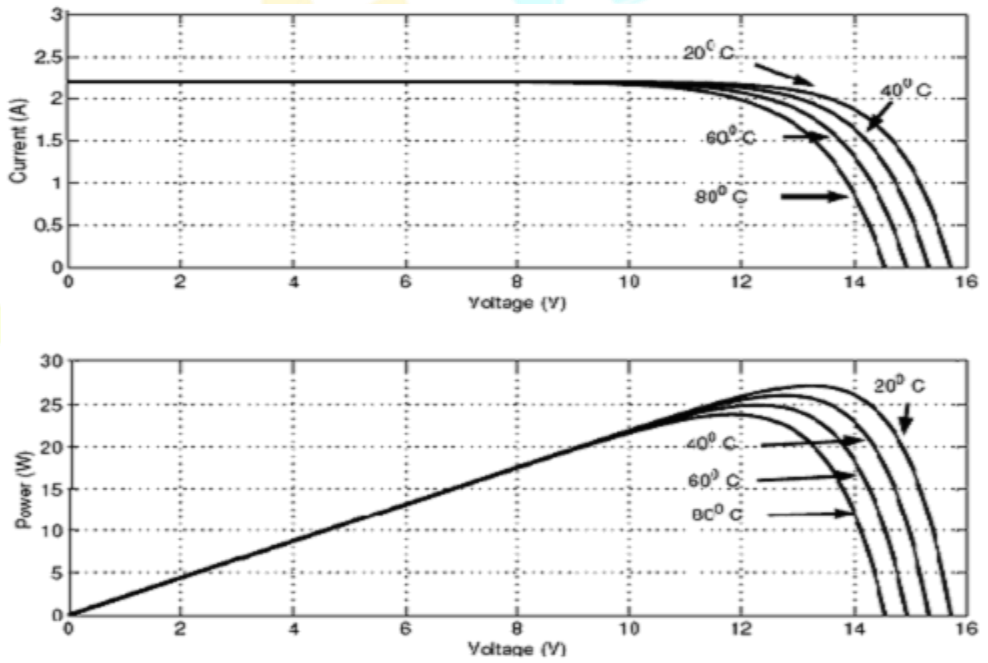


Fig.2.5: I-V and P-V Charecteristics of aSolar Cell with Varying Temperature

The band gap energy of semiconductor materials also varies with temperature. An increase in temperature will cause the band gap energy of the material to increase. With higher band gap energy, the electrons in the valence band will require more energy from the photons to move to the conduction band. This means that a lot more photons will not have sufficient energy to be absorbed by the electrons in the valence band resulting in fewer electrons making it to the conduction band and a less efficient solar cell.

It should be noted here that irradiance and temperature represent only two of the most significant external factors that affect the efficiency of a solar cell. Inclination, location and time of the year are also factors that affect the efficiency of solar cells. Additional parameters of a solar cell can be discussed by an illustration of the maximum power point as shown in Fig 2.6.

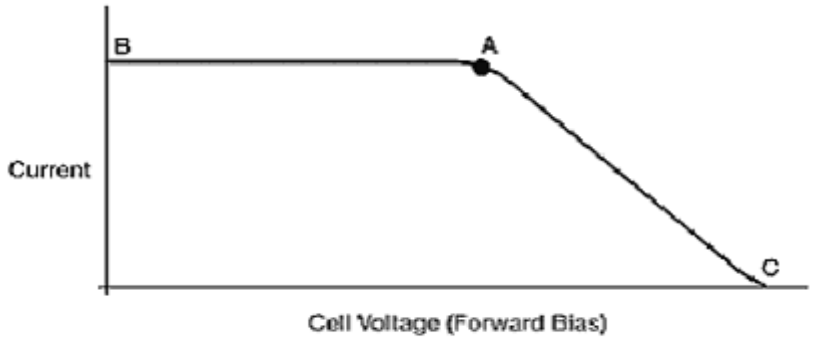


Fig.2.6: Illustration of Maximum Power Point

The cell's short circuit current intersects the Y-axis at point B and the open circuit voltage intersects the X-axis at point C. To achieve maximum energy transfer, systems powered by solar cells should be designed to transfer energy to the load at point A on the I-V curve. No energy should be delivered at points B and C, and most of the energy should be delivered as the operating point approaches point A. In a solar panel array, it is even more important that load impedance and source impedance are well matched. Once the cells are matched by their I-V characteristics, they can be grouped into individual arrays and each array is then made to operate at its maximum energy transfer point.

Majority of solar cells have high capacitance associated with their forward biased p-n junctions because the charged carriers are much closer together. The unwanted capacitance increases as the size of the solar cell and junction area increases. The I-V curve of the solar cell can be determined by taking fast I-V measurements, which is done by applying a constant voltage and measuring the resulting current for the device being tested. However the high capacitance makes it difficult to get fast I-V measurements.

The shape of the I-V curve of the solar cell is governed by the cell's high Thevenin's equivalent impedance. The short circuit current is determined by the incident light intensity and it is inversely proportional to the applied voltage. The total circuit voltage and incident light determine the external circuit current.

2.3.4 Solar Cell Modelling

To properly model a solar cell, it is important to understand how solar cells operate. Solar cells are primarily made of semiconductor material that when exposed to light induces a process of photon reflection and absorption, generation of free carriers and lastly charge separation, which creates an electric field. The semiconductor properties determine how effectively this process occurs. Some of the most important properties include the absorption coefficient, the reflectance of the semiconductor surface, drift-diffusion parameters and surface recombination velocities.

For practical power applications, the voltage produced by one solar cell is usually not sufficient to power most equipment. An array of 20 to 80 solar cells connected in series to form a "Solar Module" is usually necessary to provide the required voltage. Solar cell manufacturers provide some key parameters of a solar module in their Data Sheet. The output power is given in Wp (Watt peak), which means the module is rated at Standard Test Conditions (STC). The STC are illumination levels of 1000 W/m2 (bright sunshine), a spectrum equivalent to Air Mass 1.5 and

25°C module temperature at the test. The manufacturer's data sheet also provides the short circuit current, the current produced when the output voltage is zero and the open circuit voltage, the voltage across the output terminals when there is no current flowing in the cell.

The simplified equivalent circuit of a solar cell consists of a diode and a current source which are switched in parallel. The current source generates the photo current I_{Ph}, which is directly proportional to the solar irradiance G. The p-n transition area of the solar cell is equivalent to a diode.

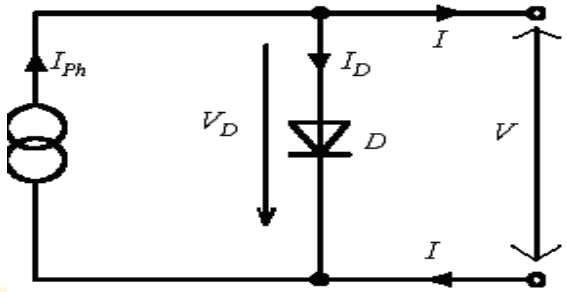


Fig.2.7: Equivalent circuit of a solar cell

The V-I *equation of the simplified equivalent circuit could be derived from Kirchhoff's current law*

$$I = I_{Ph} - I_D = I_{Ph} - I_S \cdot (\exp(\frac{V}{m \cdot V_T}) - 1) \qquad \textbf{…(2.1)}$$

Where

I_{Ph} --- *Photo current*

I_D --- *Diode current*

I_S --- *Diode reverse saturation current*

m --- Diode ideal factor

V_T = (k*T)/q is Thermal voltage (25.7 mV at 25ºC)

k = Boltzmann Constant=1.3824*e-23

T = Absolute Temperature

q = charge of an electron=1.60*e-19 couloumbs

V = output voltage of the solar cell

I = output current through the solar cells

The simplified equivalent circuit doesn't give an optimal representation of the electrical process at the solar cell. In real solar cells a voltage loss on the way to the external contacts could be observed. This voltage loss could be expressed by a series resistor R_S. Furthermore leakage currents could be observed, which could be described by a parallel resistor R_P. (Fig. 2.8)

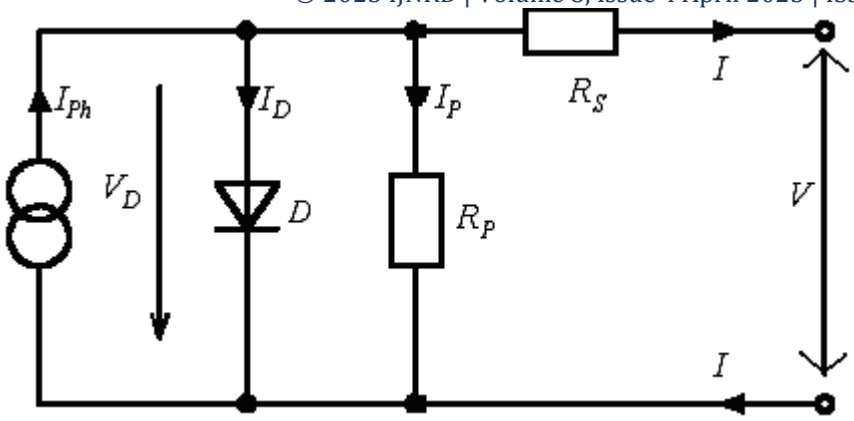


Fig.2.8: *Equivalent Circuit for One Diode Model Of A Solar Cell*

Derived from Kirchhoff´s first law the equation for the extended I-V curve could be achieved.

$$I = I_{Ph} - I_D - I_P \quad \text{... (2.2)}$$

$$I_P = V_D / R_P = \left\{ \frac{(V + IR_S)}{R_P} \right\} \quad \text{... (2.3)}$$

$$I = I_{Ph} - \left\{ I_S \left(\exp\left(\frac{q(V + IR_S)}{mkTN_S} \right) - 1 \right) \right\} - \left(\frac{V + IR_S}{R_P} \right) \quad \text{... (2.4)}$$

Where

I_{Ph} *is the photo current*

I_D *is the Diode current*

R_S is the cell's series resistance, R_P is the shunt resistance

The specifications of the solar module supplied by the manufacturer's data sheet are as shown in Table.2.1.

Table 2.1: The key specifications of the solar MSX – 60 PV panel

At Temperature T = 25°C, Insulation G=1000W/m^2		
Open circuit voltage	V_{oc}	21.0 V
Short circuit current	I_{sc}	3.74A
Voltage at max.power	V_m	17.1V
Current at max power	I_m	3.5A
Maximum power	P_m	60.0W

II. MODELLING OF PV AND DC-DC BOOST CONVERTER

A. MODELLING OF SOLAR PV

The modeling of a solar cell is an important segment of analyzing a solar PV system. The overall proposed circuit comprises solar panels, a three-level DC-DC boost converter fed to 53-level MLI shown in Figure 1. The solar PV can be modeled with three categories such as an equivalent circuit with current-voltage (I-V) and power-voltage (P-V) characteristics, the effect of solar irradiance and temperature, and

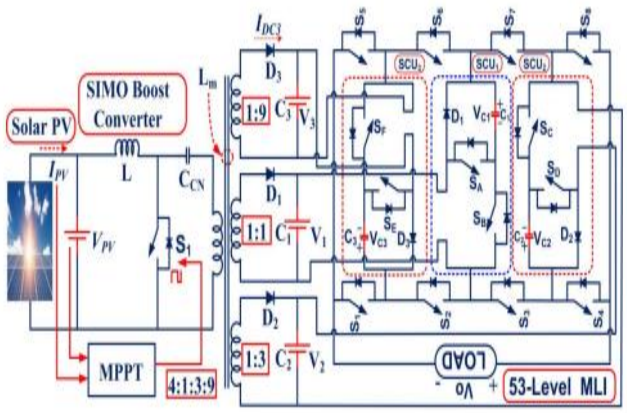


FIGURE 1. Overall structure of the 17 level system.

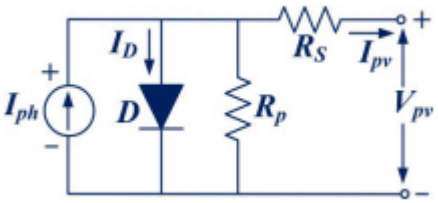


FIGURE 2. Equivalent circuit of solar cell.

the partial shading condition is taken into consideration. PV resembles two words photo and voltaic: photo represents the photonic energy and voltaic represents the electrical energy, which implies that the energy conversion from photonic energy into electrical energy [30]. The combination of a solar array is of various types of modules, where each module comprises solar cells. This comprises of p-n semiconductor diodes [31]. The designed solar PV has a behavior of changing its output with the variation of temperature and climatic conditions [32]. Therefore, the factors in modeling a solar PV are represented below:

1) Solar Cell: Equivalent Circuit And I–V Characteristics

The solar cell comprises internal resistance RSE and RSH connected to the diode in series and parallel combination, known to be an equivalent circuit shown in FIGURE 2. VPV and IPV are the output voltage and current of a solar

cell, respectively. These are got from the series and parallel connection of several PV modules shown in equation (1),

$$I_{PV} = \left\{ I_{Ph} - I_0 \left[exp\left(\frac{q(V_{PV} + R_{SE} I_{PV})}{N_{SE} AKT} \right) - 1 \right] - \frac{(V_{PV} + R_{SE} I_{PV})}{N_{SE} R_{SH}} \right\} \quad (1)$$

where NSE and NSH are the number of PV cells in series and parallel connection. RSE is the series resistance, and RH is the parallel resistance. A is the ideality factor of a semiconductor device. K is Boltzmann's constant (1.3806503 × 10−23 J/K), T is 'he temperature. Ip is the current produced and is depends

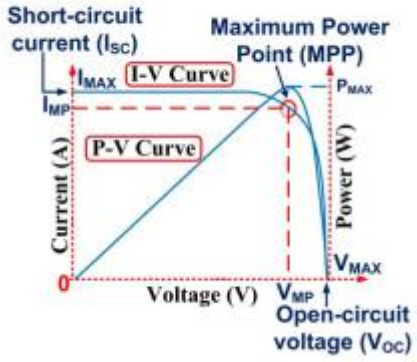


FIGURE 3. I-V Characteristics of solar cell.

$$I_P = [I_{SK-STM} + K_i (T - T_{STM})] - \left(\frac{G}{G_{STM}} \right) \quad (2)$$

where ISK−STM is a short-circuited current at standard testing cases (STM), Ki is the SCC coefficient, G (W/m2) is the irradiance on the surface of the cell, GSTM (1000W/m2) is the irradiance at STM, and the cell temperature is TSTM [33].

$$I_O = \left\{ \frac{I_{SK-STM} + K_i (T - T_{STM})}{exp\left[(V_{OK-STM} + K_{OV} (T - T_{SKC}) / AV_{Sth} \right]} \right\} \quad (3)$$

where VOK−STM is an open-circuited voltage at the standard testing case, KOV represents the open-circuit voltage coefficient, VSth is solar cell thermal voltage

$$P_{PV} = V_{PV} \times N_{SH} \left(I_{Ph} - I_O exp\left(\frac{q V_{PV}}{N_{SE} AKT} \right) - \left(\frac{V_{PV}}{N_{SE}} \right) \right) \quad (4)$$

I-V/P-V curves represent the characteristics of a solar cell is shown in FIGURE 3 [4]. It is clear from the curve there is instability for the operating point of a PV; it varies continuously from null to open-circuit voltage. In this process,

there is a single point that provides peak power for the design of solar PV at various irradiance. Here, the respective voltage and currents are VMPP, IMPP shown in Figure 3.

2) Irradiance And Temperature Effect

The solar PV output continuously varies with variation in climatic changes [34]. As the solar irradiance confides on the incidence angle of sun rays, this effect forces the I-V/PV characteristics to change. The output current IPV varies with the variation of sunray incidence, making VPV constant and VPV also shifts its magnitude, making IPV constant [34]. Three factors are influencing the variation in temperature of a solar PV: The heat dissipated on its own during the functioning of PV, for the infrared wavelength started, which is a worn on the cell and the gradual increase in the sunbeam intensity [26]. The VOC and ISC are measured based on the equations (5) and (6) at variable irradiance.

$$V_{OC} = V'_{OC} + a_2 (T - T') - (I_{SC} - I'_{SC}) R_{SE} \quad (5)$$

$$I_{SC} = I'_{SC} \left(\frac{G}{G'} \right) + a_1 (T - T') \quad (6)$$

3) Partial Shading Effect

Apart from the temperature and irradiance conditions, a partial shading case is also a challenging task for the MPPT technique in achieving maximum power. This partial shade occurs with mists, consecutive structures, trees, etc. [36]. According to equation (2), the photocurrent Iph gets reduced with low insolation. With series-connected PV modules, the current is the same in all cells. But in this case, the shaded cell goes to a breakdown, and instead of providing the energy, this acts as a load because of the weakening of photocurrent.

MAXIMUM POWER POINT TRACKING

Maximum Power Point Tracking, frequently referred to as MPPT, is an electronic system that operates the Photovoltaic (PV) modules in a manner that allows the modules to produce all

the power they are capable of. MPPT is not a mechanical tracking system that "physically moves" the modules to make them point more directly at the sun. MPPT is a fully electronic system that varies the electrical operating point of the modules so that the modules are able to deliver maximum available power. Additional power harvested from the modules is then made available as increased battery charge current. MPPT can be used in conjunction with a mechanical tracking system, but the two systems are completely different.

The problem considered by MPPT methods is to automatically find the voltage VMPP or current IMPP at which a PV array delivers maximum power under a given temperature and irradiance. In this section, commonly used MPPT methods are introduced in an arbitrary order.

A. Fractional Open-Circuit Voltage

The method is based on the observation that, the ratio between array voltage at maximum power VMPP to its open circuit voltage VOC is nearly constant.

$$V_{MPP} \approx k_1 V_{OC}$$

This factor k1 has been reported to be between 0.71 and 0.78. Once the constant k1 is known, VMPP is computed by measuring VOC periodically. Although the implementation of this method is simple and cheap, its tracking efficiency is relatively low due to the utilization of inaccurate values of the constant k1 in the computation of VMMP.

B. Fractional Short-Circuit Current

The method results from the fact that, the current at maximum power point IMPP is approximately linearly related to the short circuit current ISC of the PV array.

$$I_{MPP} \approx k_2 I_{SC}$$

Like in the fractional voltage method, k2 is not constant. It is found to be between 0.78 and 0.92. The accuracy of the method and tracking efficiency depends on the accuracy of K2 and periodic measurement of short circuit current.

C. Perturb and Observe

In P&O method, the MPPT algorithm is based on the calculation of the PV output power and the power change by sampling both the PV current and voltage. The tracker operates by periodically incrementing or decrementing the solar array voltage. If a given perturbation leads to an increase (decrease) in the output power of the PV, then the subsequent perturbation is generated in the same (opposite) direction. So, the duty cycle of the dc chopper is changed and the process is repeated until the maximum power point has been reached. Actually, the system oscillates about the MPP. Reducing the perturbation step size can minimize the oscillation. However, small step size slows down the MPPT. To solve this problem, a variable perturbation size that gets smaller towards the MPP.

However, the P&O method can fail under rapidly changing atmospheric conditions. Several research activities have been carried out to improve the traditional Hill-climbing and P&O methods. A three-point weight comparison P&O method that compares the actual power point to the two preceding points before a decision is made about the perturbation sign. Reference proposes a two stage algorithm that offers faster tracking in the first stage and finer tracking in the second stage.

D. Incremental Conductance

The method is based on the principle that the slope of the PV array power curve is zero at the maximum power point.

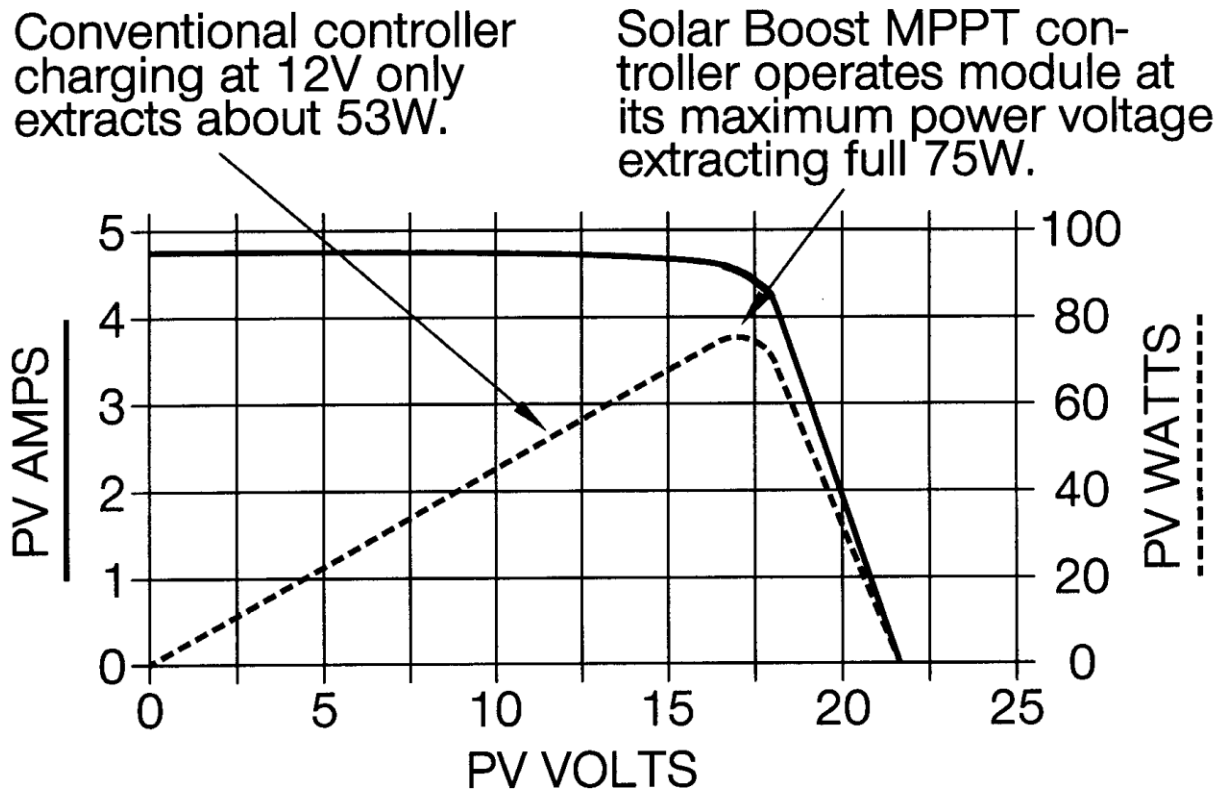
(dP/dV) = 0. Since (P = VI), it yields:

$$\Delta I/\Delta V = -I/V \text{ , at MPP}$$
$$\Delta I/\Delta V > -I/V \text{ , left of MPP}$$

$\Delta I/\Delta V < -I/V$, right of MPP

The MPP can be tracked by comparing the instantaneous conductance (I/V) to the incremental conductance (ΔI/ΔV). The algorithm increments or decrement the array reference voltage until the condition of equation (4.a) is satisfied. Once the Maximum power is reached, the operation of the PV array is maintained at this point. This method requires high sampling rates and fast calculations of the power slope.

To understand how MPPT works, let's first consider the operation of a conventional (non-MPPT) charge controller. When a conventional controller is charging a discharged battery, it simply connects the modules directly to the battery. This forces the modules to operate at battery voltage, typically not the ideal operating voltage at which the modules are able to produce their maximum available power. The PV Module Power/Voltage/Current graph shows the traditional Current/Voltage curve for a typical 75W module at standard test conditions of 25°C cell temperature and 1000W/m2 of insulation. This graph also shows PV module power delivered vs module voltage. For the example shown, the conventional controller simply connects the module to the battery and therefore forces the module to operate at 12V. By forcing the 75W module to operate at 12V the conventional controller artificially limits power production to »53W.

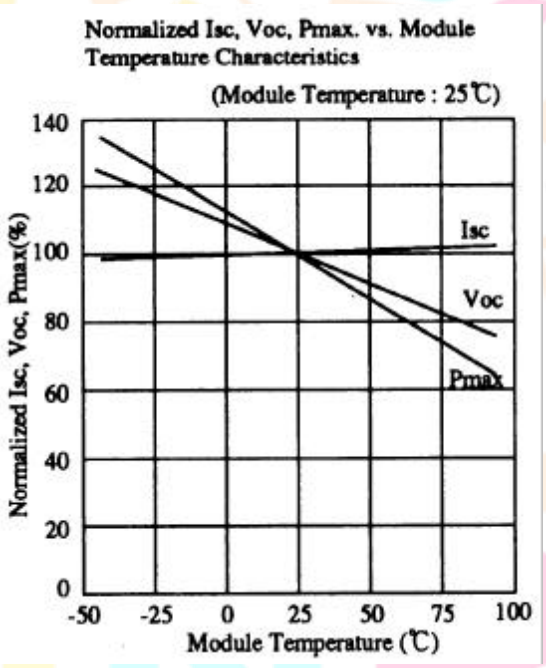


Rather than simply connecting the module to the battery, the patented MPPT system in a

Solar Boost charge controller calculates the voltage at which the module is able to produce maximum power. In this example the maximum power voltage of the module (VMP) is 17V. The MPPT system then operates the modules at 17V to extract the full 75W, regardless of present battery voltage. A high efficiency DC-to-DC power converter converts the 17V module voltage at the controller input to battery voltage at the output. If the whole system wiring

and all was 100% efficient, battery charge current in this example would be VMODULE ¸ VBATTERY x IMODULE, or 17V ¸ 12V x 4.45A = 6.30A. A charge current increase of 1.85A or 42% would be achieved by harvesting module power that would have been left behind by a conventional controller and turning it into useable charge current. But, nothing is 100% efficient and actual charge current increase will be somewhat lower as some power is lost in wiring, fuses, circuit breakers, and in the Solar Boost charge controller.

Actual charge current increase varies with operating conditions. As shown above, the greater the difference between PV module maximum power voltage VMP and battery voltage, the greater the charge current increase will be. Cooler PV module cell temperatures tend to produce higher VMP and therefore greater charge current increase. This is because VMP and available power increase as module cell temperature decreases as shown in the PV Module Temperature Performance graph. Modules with a 25°C VMP rating higher than 17V will also tend to produce more charge current increase because the difference between actual VMP and battery voltage will be greater. A highly discharged battery will also increase charge current since battery voltage is lower, and output to the battery during MPPT could be thought of as being "constant power".



III MPPT CONTROLLER

The operating of solar PV is to extract the maximum power from the PV module is an MPPT controller. During all the disturbances mentioned above, if the controller can able to operate efficiently in tracking and to provide peak power from the solar panels, the efficiency and life span of the

TABLE 1. Specifications of the 215W PV system.

Maximum power	213.15W
The voltage at maximum power point (V_{MPP})	29V
Open circuit voltage (V_{oc})	36.3V
Current at maximum power point (I_{MPP})	7.35A
Short circuit current (I_{sc})	7.84A
Diode ideality factor	0.98117
Diode saturation current (I_O)	2.9259×10^{-10}A

S olar PV gets increased. This can be achieved by sinking the solar source to the load for various climate conditions to produce maximum power. There are two ways to extracting the maximum power from a solar panel. They are Mechanical and electrical tracking. With mechanical tracking, the solar panels change their direction depends on the climatic variation patterns. This includes seasonal climate changes for several months. With electrical tracking, the I-V curve is forced to locate the point of maximum power in the operation of the PV array [37]. The MPPT controller is an internal part of the system which feeds the maximum power to load (batteries/motors). For tracking maximum power during the operation of the PV module, a suitable algorithm is to be used. This can be seen in the P-V graph of a solar cell. There are many such methods to track the maximum power such as incremental conductance, perturb and observe, genetic algorithm, fractional open-circuit voltage, etc. In this paper, the perturb and observe algorithm it has many advantages. It is easy to implement using various controllers such as Arduino, microcontroller, etc. The maximum power point determination speed can be controlled by varying the perturbation value. The P&O algorithm is shown in Figure 4. The algorithm for Perturb and Observe Technique is:

a) Ipv and Vpv values are gathered from PV module.

b) Ppv is calculated from Ipv and Vpv.

c) Voltage and power values are stored.

d) The values are recorded for the next consecutive (k + 1)th instant and repeat step ‘a’.

e) The values got at (k + 1)th instant are subtracted from the values got at kth instant.

f) In the PV curve of a solar panel, on the right side, the slope is negative i.e., (dP/dV0). Therefore, the lesser duty cycle occurs on the right side of the curve and the high-duty occurs on the left side of the curve.

g) Based on the polarity of the slope after subtraction, the algorithm decides the change in the duty cycle. The solar panel is designed with a power of 215W; the respective parameters and their specifications are shown in TABLE 1.

Dc-Dc Boost Converter

A Single Input Multiple Output DC-DC Boost Converter InterFaced In Between The Solar Panels And The Proposd

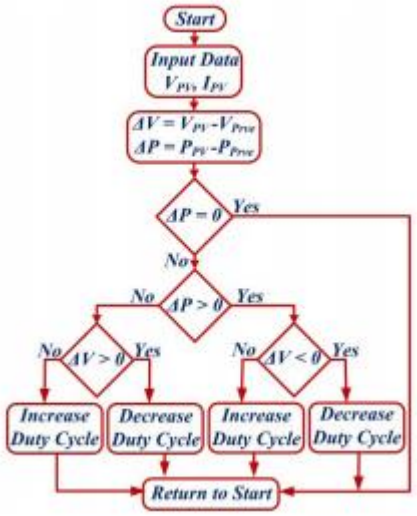


FIGURE 4. Flowchart of P&O algorithm.

$$L = \left(\frac{mV_{dc}}{4af_sI_r}\right) \quad (7)$$

$$C = \left(\frac{DI_{dc}}{V_{dc}rf_s \times 0.5}\right) \quad (8)$$

$$D = \left(\frac{V_O}{V_O + V_{dc}}\right) \quad (9)$$

CHAPTER-3

POWER ELECTRONIC CONVERTERS

3.1 Introduction

Inverters have been developed over the last three decades for the purpose of meeting the drive high voltage rating and low dv/dt value requirements that could not be met by the classical two-level inverter. Until recently, power transistors were slow, and their long turn-on and off times resulted in excessive switching losses that constrained the switching frequency to several kHz values. Also the voltage blocking capability of power transistors was below a kilovolt that implied such switches could not be utilized in two-level inverters at high voltage levels and could not be operated at switching frequencies in the tens of kilohertz range.

3.1.1 Introduction GTO

In the early 1980's utilizing darling ton power transistors and Gate Turn Off Thyristors (GTOs), the three-level NPC inverter could provide effectively quadrupled switching frequency and could provide high inverter voltage ratings

(twice that of the two-level inverter). As a result, power and voltage levels above that of two-level inverter could be reached and the three-level NPC inverter has found immediate application in traction drives and industrial drives.

3.1.2 Introduction IGBT

In the 1990's, the IGBT was introduced as a fast turn-on, fast turn-off device that provided significant switching loss reduction and also the secondary breakdown of the Bipolar Junction Transistor (BJT) was absent. As a result, IGBTs with higher switching frequencies and blocking voltages have extended the two-level inverter ratings to the kilovolt level and some of the three-level NPC inverter applications could be replaced with the two-level inverter. However, in particular in the 400 V and above voltage levels, the two-level inverter turned out to be problematic in terms of the dv/dt stresses during the fast switching of IGBTs. As a result, the NPC inverter has been favored again due to its reduced dv/dt rating compared to the two-level inverter. As a result at 400 V and above, when fast IGBTs are utilized it is presently favorable to utilize the three-level NPC inverter.

At the present time, as the power converter rating increases above a megawatt, which also implies a voltage rating above 400 V, the practical power converter topology is a multilevel inverter topology. In the lower megawatt range the three levels NPC inverter and at the higher range the cascaded H-bridge topology have been in use in industry for longer than a decade.

Utility power electronics applications such as Static Compensator (STATCOM), Unified Power Flow Controller (UPFC), and Flexible AC Transmission System (FACTS) applications involve higher level inverters such as four, five or higher level NPC inverters and recently the flying capacitor topology has also been considered.

In the utility power electronics applications, multilevel inverters are required because the voltage levels involved are very high (kV range) and the required level can only be reached by either series connection of large number of power semiconductor or by means of multilevel inverter topologies involving large number of levels. At the 400 V distribution system level, generally the three-level inverter topology suffices.

3.2 TYPES OF Multilevel inverters

In general, multilevel inverter topologies synthesize variable frequency variable voltage that is nearly sinusoidal output waveform with low dv/dt, reduced common mode voltage, and low harmonics yielding a motor friendly performance. Although the topology types are various, in all multilevel inverter topologies the basic idea is to utilize low voltage rating power transistors in series connection along with multistage DC capacitor voltage levels such that higher output voltage levels with small incremental steps could be obtained.

With high voltage waveform quality, the multilevel inverters result in negligible bearing current and decrease the effect of winding insulation breakdown in motor drives. Due to the reduced stresses and EMI, they provide better interface between DC voltage sources/loads and the AC utility grid when operated as PWM rectifiers and power conditioners.

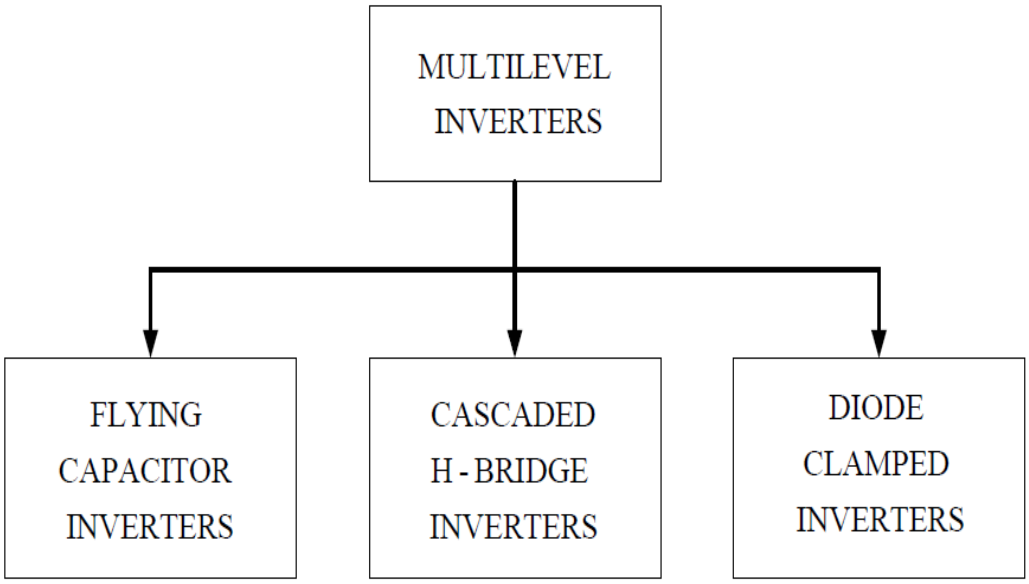


Fig: 3.1 multilevel inverter topologies.

In multilevel inverters, to increase the number of output voltage levels, the number of semiconductor devices and capacitor voltage sources should be increased. As a result, the power and control circuit of the multilevel inverter becomes more complex, large and costly. In addition, significant voltage imbalance problems arise. Therefore, with the three-level inverter being the most common, mainly up to five-level inverters has been reported. The topology option is more constrained than the number of levels. As illustrated in Figure 3.1, multilevel inverter technology involves three different topological structures.

3.2.1 FLYING CAPACITOR MULTILEVEL INVERTER TOPOLOGY

The flying capacitor multilevel inverter topology was proposed in 1992. The flying capacitor topology is also called as "capacitor clamped multilevel inverter." Fig 3.2.a shows one phase leg of the three-level version of this topology and Fig 3.2.b shows corresponding output voltage waveform when switching at the fundamental frequency. The five-level flying capacitor inverter circuit topology and its output voltage waveform are shown in Fig 3.3.a and Fig 3.4.b, respectively. With all capacitor voltages being equal, in the three-level flying capacitor inverter, the output voltage V_{U0} has three different voltage levels –Vdc/2, 0, and +Vdc/2. For the voltage level +Vdc/2 the semiconductor switches SU1 and SU2 have to be turned ON. For the 0 level, semiconductor switches SU1 and SU3 or SU2 and SU4 need to be turned ON. For –Vdc/2, semiconductor switches SU3 and SU4 need to be turned ON. For the five-level case the same strategy can be used to obtain five-level output voltage waveform.

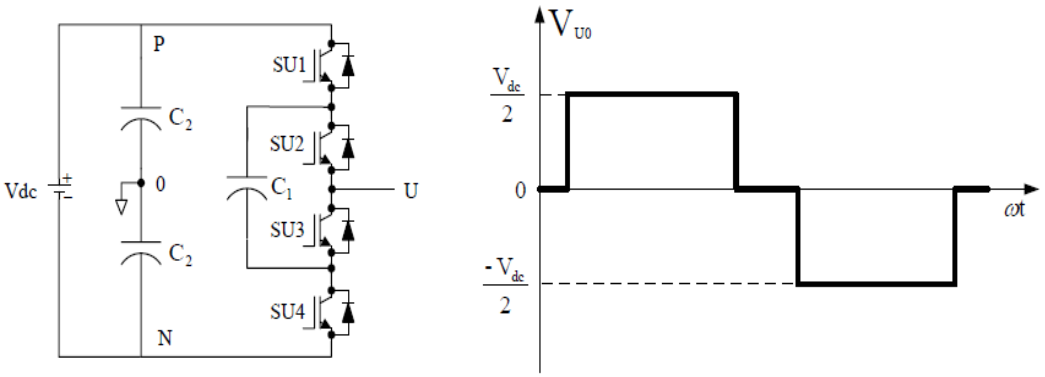


Fig: 3.2 Three-level flying capacitor inverter phase leg structure (a) and output voltage waveform (b).

The capacitor charge control method of the flying capacitor inverter topology is complex and the required control algorithm to maintain capacitor voltages within a specified range is involved. The flying capacitor topology requires larger capacitors (the flying capacitors) than the diode-clamped multilevel inverter DC bus capacitors. Therefore, the flying capacitor topology is not feasible for ASD systems and has mainly been considered for utility power electronics applications.

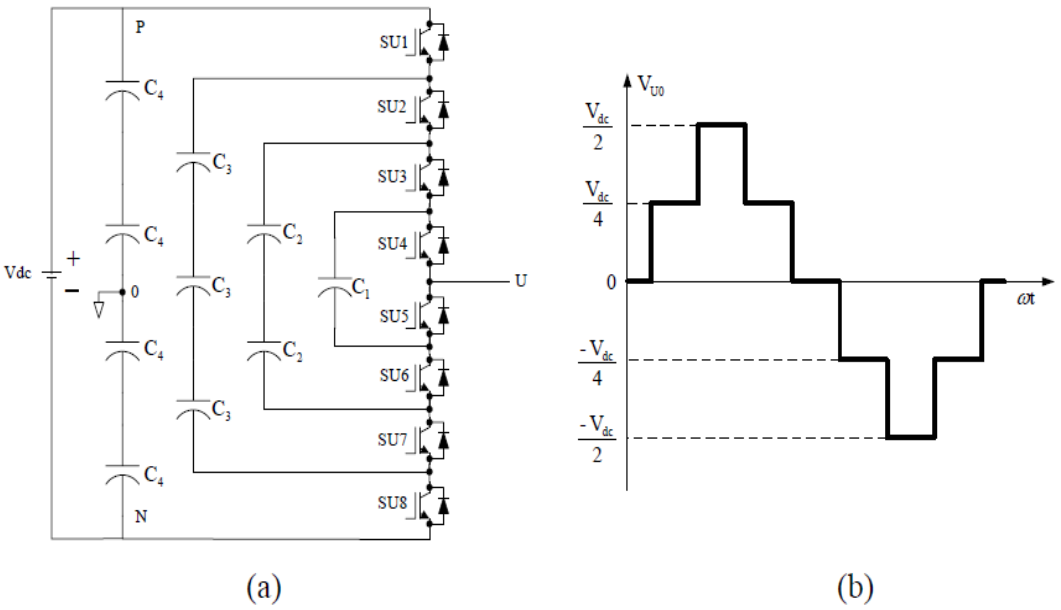


Fig: 3.3 Five-level flying capacitor inverter phase leg structure (a) and output voltage waveform (b).

3.2.2 CASCADED H-BRIDGE MULTILEVEL INVERTER TOPOLOGY

In the cascaded H-bridge inverter topology, single phase H-bridge inverters with isolated (separate) DC sources are connected in series. Each such unit is called a cell. Figure 3.4.a shows one phase of the five-level cascaded H-bridge inverter topology and Figure 3.4.b shows the output voltage waveform. This topology has been utilized in industry for medium voltage motor drive applications. Each single-phase H-bridge inverter generates three voltage levels at the output: -Vdc, 0, and +Vdc. This is made possible by connecting the capacitors sequentially to the AC side via semiconductor switches. In the five-level cascaded inverter, two cells per-phase are connected in series as

shown in Figure 3.4.a. Of the two cells of a phase, in each cell, the DC bus voltage can be different provided that in each phase the same level cell has the same voltage. Then various voltage step waveforms could be obtained. In the case that the voltage levels of all cells are the same, the analysis and synthesis becomes simple. In this case, depending on the output voltage of each cell, the phase output voltage can be one of the following discrete levels; 2Vdc, -Vdc, 0, +Vdc, +2Vdc.

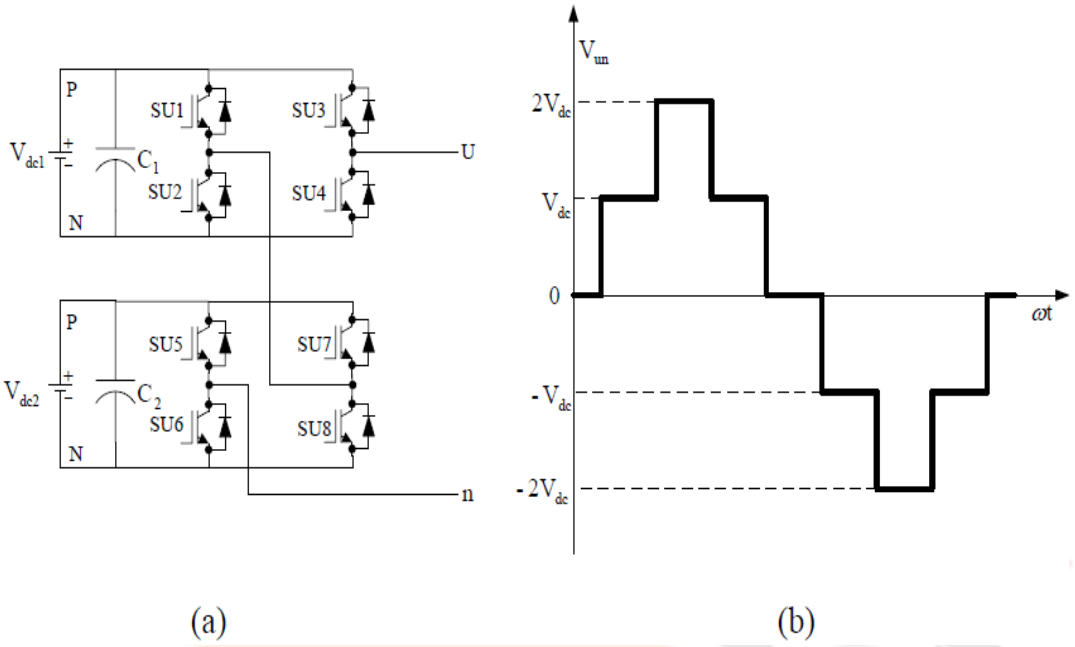


Fig: 3.4 the structure of one phase leg of the five-level cascaded multilevel inverter (a) and its output voltage waveform (b).

The cascaded H- bridge multilevel inverter topology has low harmonic content at the motor terminal voltages and low dv/dt rating. By selecting various DC bus voltage levels for various cells and also by selecting a sufficiently large cell count, it is possible to obtain high output voltage waveform quality even at very high voltage and power levels. The cascaded H-bridge inverter topology is fault tolerant. A fault in a single-phase inverter does not necessitate complete shutdown of the ASD system. This structure has modularity, and for this reason maintenance is easy. Isolated DC voltages could be provided via multi winding transformers and with appropriate rectifier and transformer design the drive AC input current waveform could be made of high quality yielding a utility line friendly performance. However, the cascaded H-bridge inverter topology involves a relatively large number of isolated H-bridge modules, a fairly large and complex input transformer, and moreover complex control circuitry. As a result, the topology is utilized in megawatt power rating motor drives. At power ratings below megawatt, the topology is prohibitive in terms of cost and complexity.

3.2.3 DIODE CLAMPED MULTILEVEL INVERTERS

As the first practical multilevel inverter topology, the three-level neutral point clamped (NPC) voltage source inverter was invented by Nabae, et al, in 1980 . Figure 3.5.a shows one phase leg of this topology and Figure 3.5.b shows its output voltage waveform. The NPC inverter is also called as the “Three-Level Diode Clamped” NPC inverter. In the topology, the DC bus voltage must be split in two via series connected capacitor banks. In the three-

level inverter, the output voltage V_{U0} has three levels; $-V_{dc}/2$, 0, and $+V_{dc}/2$. For $+V_{dc}/2$ semiconductor switches S_{U1} and S_{U2} are turned ON. For 0 output voltage, semiconductor switches S_{U2} and S_{U3} are turned ON. And for $-V_{dc}/2$ semiconductor switches S_{U3} and S_{U4} are turned ON. The semiconductor switches (SU1, SU3) and (SU2, SU4) are turned ON and OFF in complementary logic. The clamping diodes DU1 and DU2 clamp the semiconductor switch voltage to half of the DC bus voltage.

In three-phase inverter, the NPC inverter phase output voltage levels and the line-to-line output voltage levels are related with the 2n-1 relation. The number of voltage levels of the line to line output voltage waveform is 2n-1, where n is the number of the phase voltage output levels. Therefore, for the three17 level NPC inverter case line-to-line output voltage consists of five different voltage levels. The three-level NPC inverter structure was originally developed for the purpose of increasing the power ratings of power converters (to megawatt levels) without paralleling or in series connecting converter modules or semiconductor devices. Since its invention the NPC inverter has found place in significant number of applications involving high voltage and/or power ratings

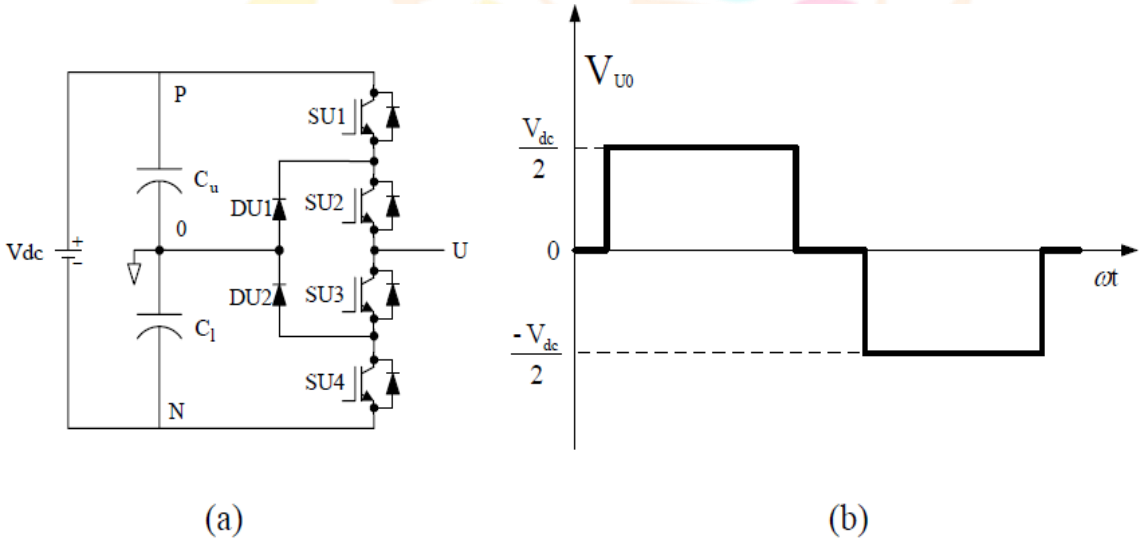


Fig: 3.5. The three-level diode clamped inverter phase leg structure (a) and output voltage waveform (b).

Although the early applications involved niche areas such as railway drives, presently the utilization has spread to the general purpose ASD area. The three-level diode clamped inverter (NPC) inverter has been utilized in 400 V and above voltage ratings in the power range from a few kilowatts to megawatt. This wide range places the three-level NPC inverter in a special place among all the multilevel inverter topologies. Similar to the flying capacitor topology, the three-level NPC inverter topology also has the drawback of capacitor voltage variation. In the three-level NPC inverter the neutral point (connection point of the two DC bus capacitors) potential may drift or vary and countermeasures must be taken when employing this topology.

3.3 Cascaded Multilevel Inverters

The smallest number of voltage levels for a multilevel inverter using cascaded inverter with SDCSs is three. To achieve a three-level waveform, a single full-bridge inverter is employed. Basically, a full-bridge inverter is known

as an H-bridge cell, which is illustrated in Fig. 3.6. The inverter circuit consists of four main switches and four freewheeling diodes.

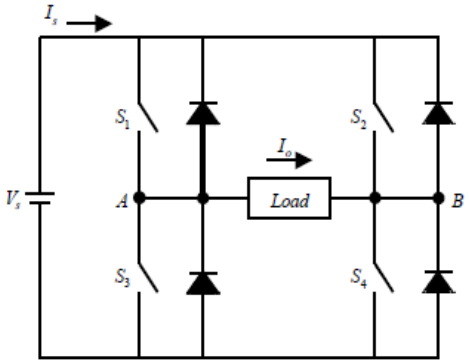


Figure 3.6 An H-bridge cell.

3.3.1 Gate Signal and Inverter Operation

According to four-switch combination, three output voltage levels, +V, -V, and 0, can be synthesized for the voltage across A and B. During inverter operation shown in Fig. 3.6, switch of S1 and S4 are closed at the same time to provide V_{AB} a positive value and a current path for Io. Switch S2 and S4 are turned on to provide V_{AB} a negative value with a path for Io. Depending on the load current angle, the current may flow through the main switch or the freewheeling diodes. When all switches are turned off, the current will flow through the freewheeling diodes.

In case of zero level, there are two possible switching patterns to synthesize zero level, for example, 1) S1 and S2 on, S3 and S4 off, and 2) S1 and S2 off and S3 and S4 on. A simple gate signal, repeated zero-level patterns, is shown in Fig. 3.7. All zero levels are generated by turning on S1 and S2.

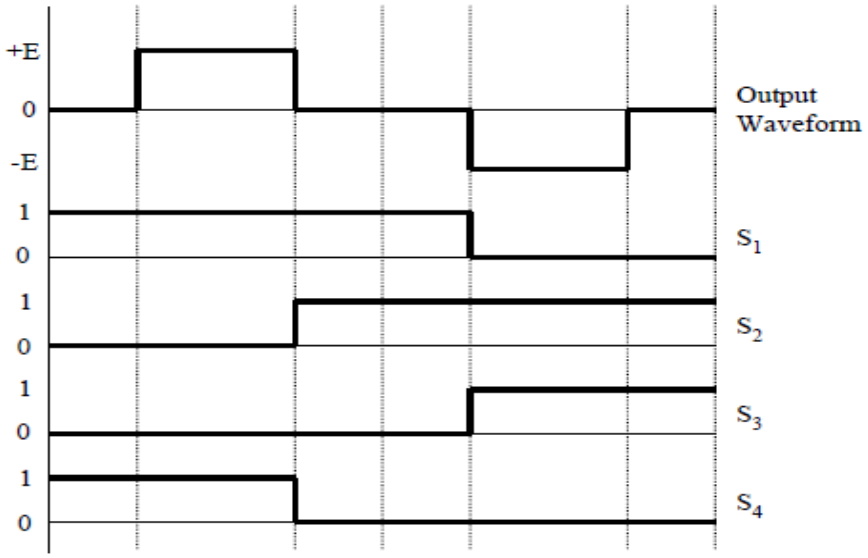


Figure 3.7 Repeated zero-level switching pattern

Note that level 1 represents the state when the gate is turned on, and level 0 represents the state when the gate is turned off. In Fig. 3.6, S1 and S2 are turned on longer than S3 and S4 do in each cycle because the same zero level switching pattern is used. As a result, S1 and S2 are consuming more power and getting higher temperature than the other two switches. To avoid such a problem, a different switching pattern for zero level is applied. In the first zero

stage, S1 and S2 are turned on; then, in the second zero stage, S3 and S4 are turned on instead of S1 and S2. By applying this method, turn-on time for each switch turns out to be equal, a shown in Fig. 3.8. This switching pattern will be used for experimental verification in this thesis.

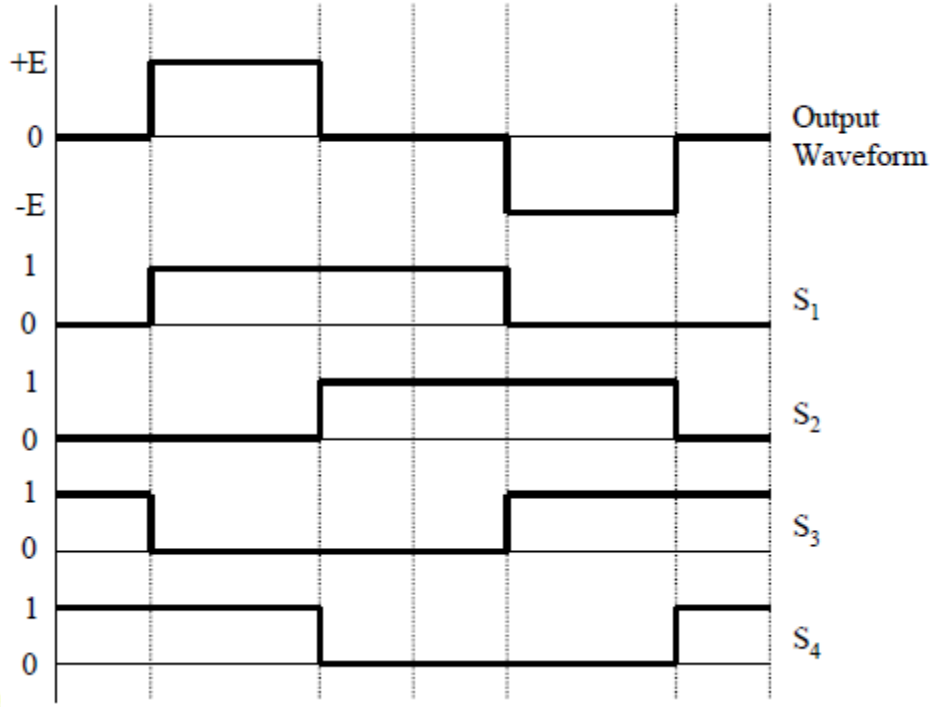


Figure: 3.8 Swapped zero-level switching pattern

3.3.2 Blanking Time

Another issue that has to be concerned is providing blanking time for gate signal. In the switches were assumed to be ideal, which allowed the state of the two switches in an inverter leg to change simultaneously from on to off and vice versa. In practice, switching devices are not ideal. To completely turn-off the devices, a short period, which depends on the type of the device, is needed. Usually, because of the finite turn-off and turn-on times associated with any types of switch, a switch is turned off at the switching time instant. However, the turn-on of the other switching in that inverter leg is delayed by a blanking time, t_D, which is conservatively chosen to avoid cross conduction current through the leg. A blanking time concept is illustrated in Fig 3.9. The leg of S1 and S3 are used as an example.

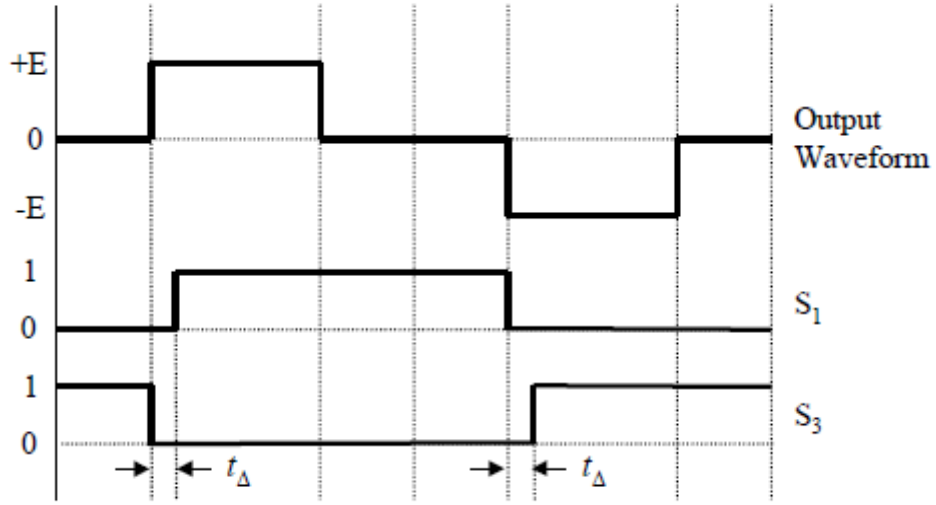


Figure: 3.9 Apply blanking time to the gate signal.

3.4 Cascade Inverter Configuration

3.4.1 Single-Phase Structure

To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

$$m = 2s + 1 \quad \text{where } s \text{ is the number of dc sources} \qquad \text{.... (3.1)}$$

For example, a nine-level output phase voltage waveform can be obtained with four-separated dc sources and four H-bridge cells. Fig 3.10 shows a general single-phase *m*-level cascaded inverter.

From Fig. 3.10, the phase voltage is the sum of each H-bridge outputs and is given as

$$V_{AN} = V_{dc1} + V_{dc2} + \ldots + V_{dc(S-1)} + V_{dc}S \qquad \text{....(3.2)}$$

Because zero voltage is common for all inverter outputs, the total level of output voltage waveform becomes $2s+1$. An example phase voltage waveform for a nine-level cascaded inverter and all H-bridge cell output waveforms are shown in Fig. 3.11. In this thesis, all dc voltage is assumed to be equal, i.e., $V_{dc1} = V_{dc2} = \ldots = V_{dc(S-1)} = V_{dc}S$

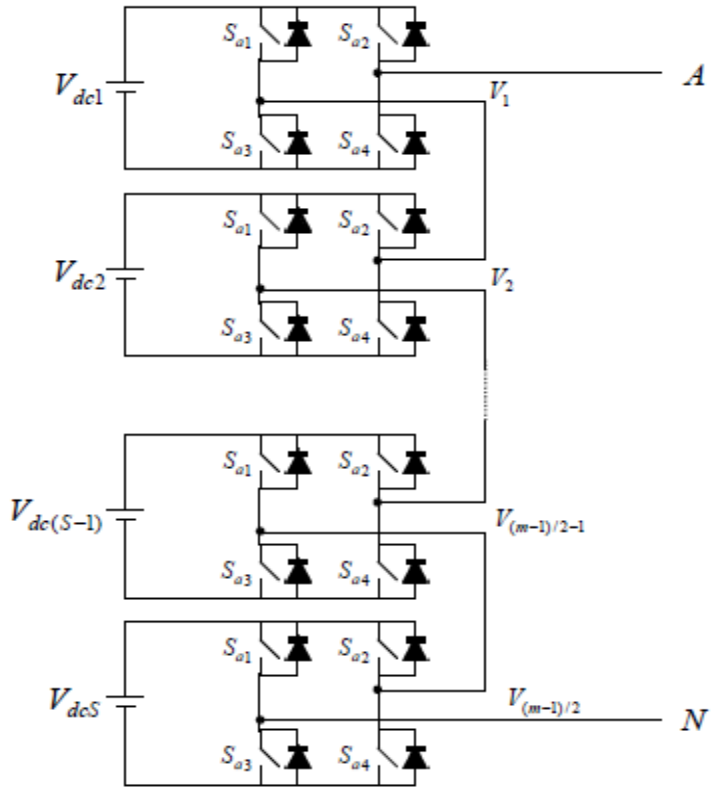


Figure 3.10 Single-phase configuration of an m-level cascaded inverter.

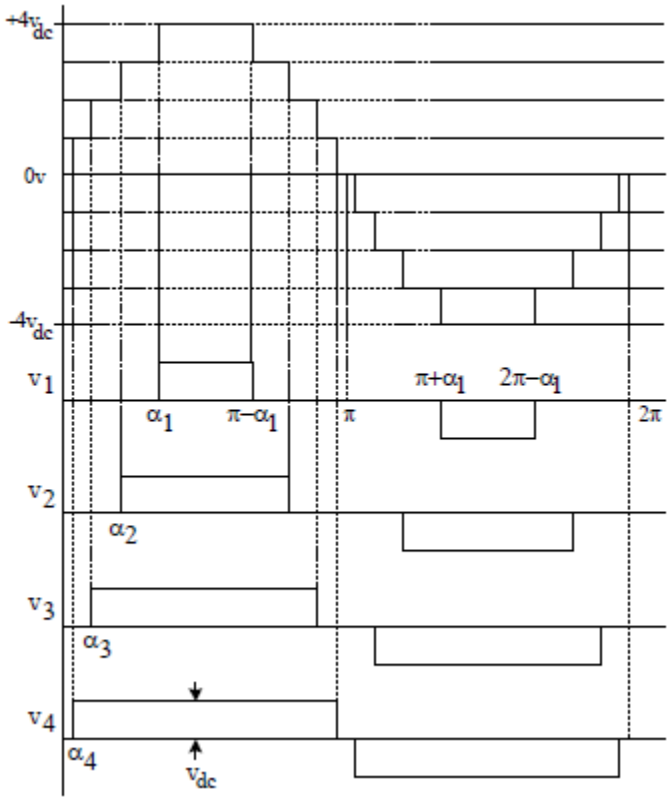


Figure 3.11 Waveform showing a nine-level output phase voltage and each H-bridge output voltage.

According to sinusoidal-liked waveform, each H-bridge output waveform must be quarter-symmetric as illustrated by V1 waveform in Fig. 3.11. Obviously, no even harmonic components are available in such a waveform. To minimize THD, all switching angles will be numerically calculated, which will be proposed.

3.4.2 Three-Phase Structure

For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either wye or delta configuration. Fig 3.12 illustrates the schematic diagram of wye-connected seven-level inverter using three H-bridge cells and three SDCSs per phase, which will be used to verify the concept of the optimized harmonic stepped-waveform technique.

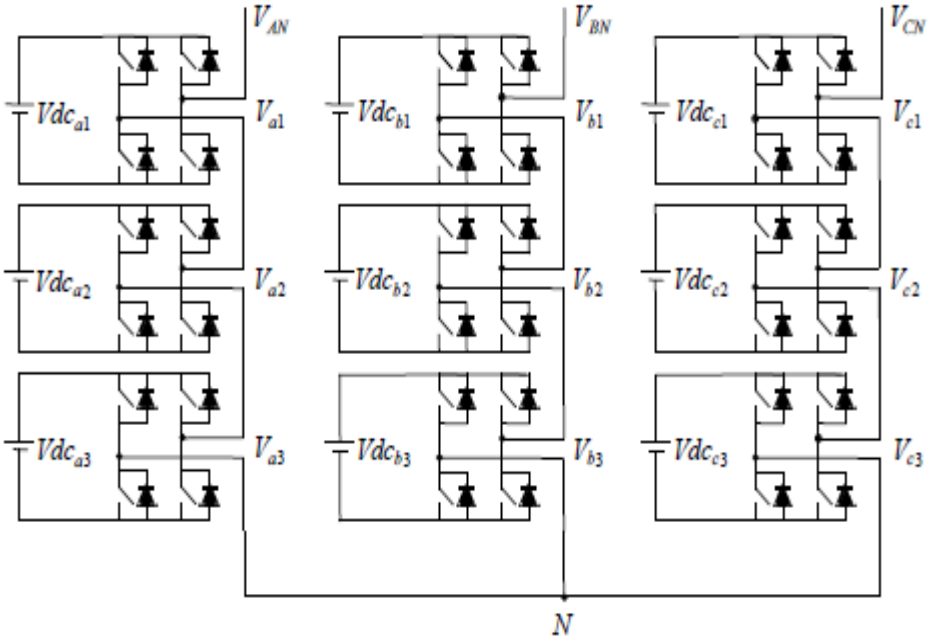


Figure:3.12 Three-phase seven-level inverter using cascaded-inverters with SDCSs.

From Fig 3.12, V_{AN} is voltage of phase A, which is the sum of V_{a1}, V_{a2}, and V_{a3}. The same idea is applied to phase B and phase C. To synthesize seven-level phase voltage, three firing angles are required. The same three switching angles can be used in all three phase with delaying 0, 120, and 240 electrical degree for phase A, B, and C, respectively.

According to three-phase theory, line voltage can be expressed in term of two phase voltages. For example, the potential between phase A and B is so-called V_{AB}, which can be written as follows:

$$V_{AB} = V_{AN} - V_{BN} \quad \text{.....(3.3)}$$

Where

V_{AB} is line voltage

V_{AN} is voltage of phase A with respect to point N

V_{BN} is voltage of phase B with respect to point N

Theoretically, the maximum number of line voltage levels is 2m-1, where m is the number of phase voltage levels. The number of line voltage level depends on the modulation index and the given harmonics to be eliminated. The seven-level cascaded inverter, for example, can synthesize up to thirteen-level line voltage.

The advantage of three-phase system is that all triplen harmonic components in the line voltage will be eliminated by one-third cycle phase shift feature. Therefore, only non-triplen harmonic components need to be eliminated from phase voltage. In single phase nine-level waveform, for example, the 3rd, 5th, and 7th harmonics will be eliminated

from output phase voltage. Compared to single-phase inverter, in three-phase nine-level inverter, the 5^{th}, 7^{th}, and 11^{th} harmonics will be eliminated from output phase voltage. Thus, the 9^{th} harmonic is the lowest harmonic component in phase voltage in single phase system, while the 13^{th} harmonic is the lowest harmonic component appearing in line voltage of three-phase system.

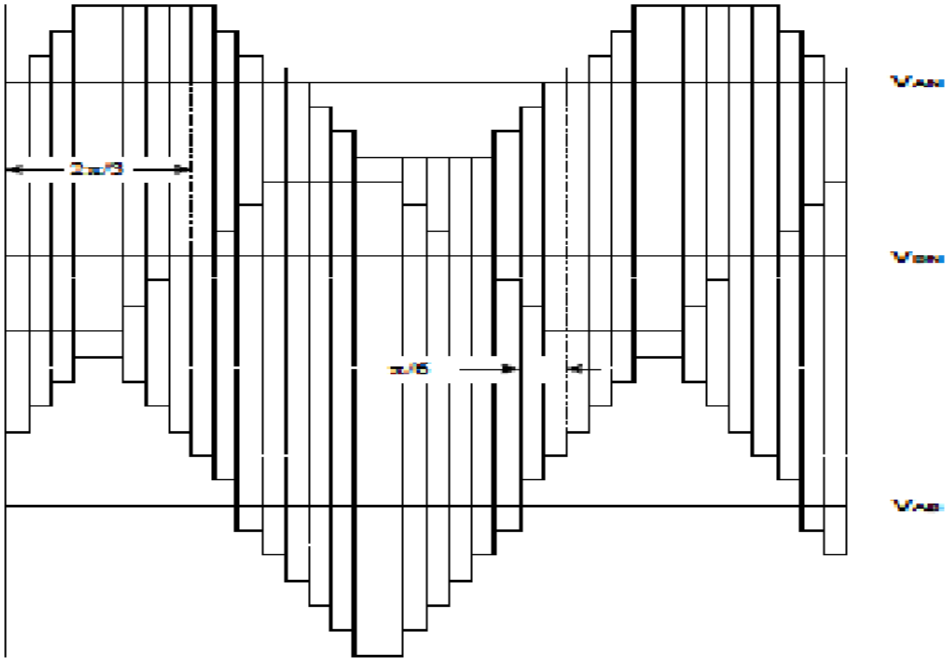


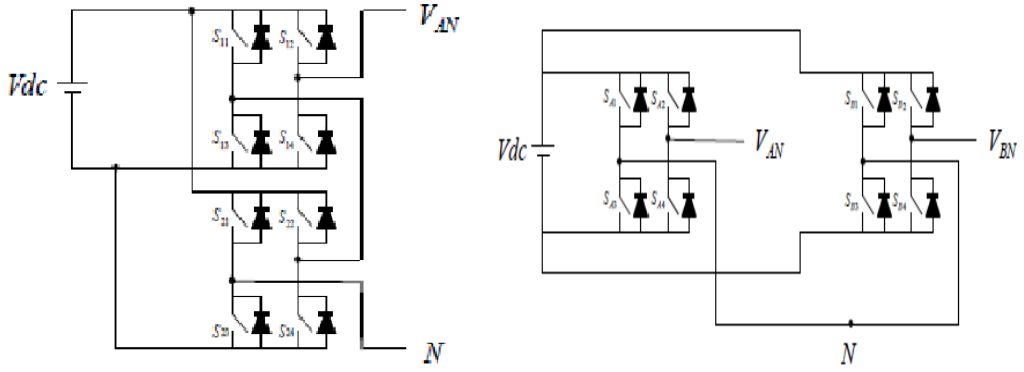
Figure 3.13 Two phase and line voltages of three-phase seven-level cascaded inverter in Fig. 3.12.

Fig 3.13 shows output voltage of phase A, V_{AN}, and output voltage of phase B, V_{BN}, line voltage waveform, V_{AB} of seven-level cascaded inverter in Fig 3.12.

From Fig. 3.13, assuming the positive sequence three-phase system, output voltage of phase B lags output voltage of phase A by 120 electrical degree. The line voltage, V_{AB}, therefore, leads voltage of phase A by 30 electrical degree, which is according to the three-phase theory.

3.4.3 Separated DC Sources (SDCSs)

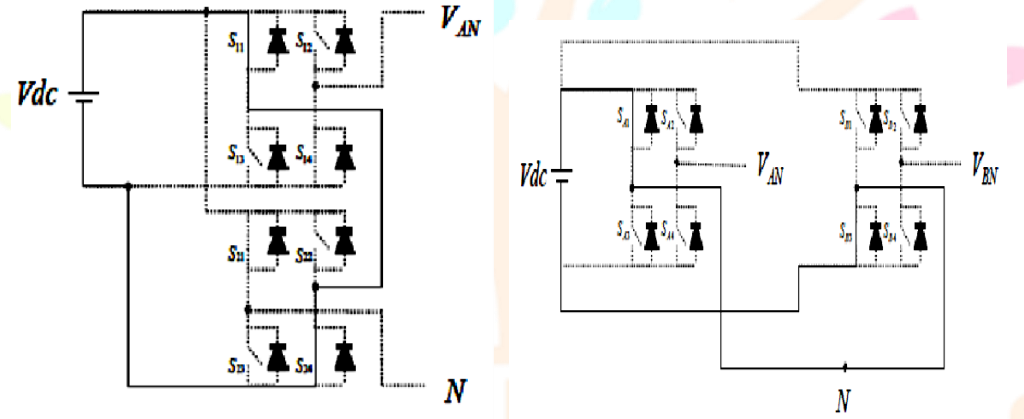
To avoid short circuit of dc sources, the separated dc source configuration is applied to the multilevel inverter using cascaded-inverter. This section will discuss about why cascaded inverter have to employ the separated dc sources (SDCSs). To explain this, two possible dc sources connections are assumed. In the first case, all H-bridge cells in the same leg share the same dc source. Another connection is that the same dc source is shared in the same level of each phase. Fig. 3.14(a) and 3.14(b) illustrate the first connection and the second connection of five-level cascaded inverter, respectively.



(a) (b)

Figure 3.14 shows two possible dc source connections

To avoid confusing, both cases will be assumed that no self shoot-through described in 1.2 is possible. However, there are many combinations, which make short circuit happen. Therefore, one possibility of each case will be presented. In the first case, short circuit across the dc source exists when switches S_{11} and S_{24} are turned on simultaneously, which is illustrated in Fig. 3.15(a). Likewise, in the second connection, when switch S_{A1} and S_{B3} are on at the same time, which is shown in Fig. 3.15(b), short circuit will be happened.



(a) (b)

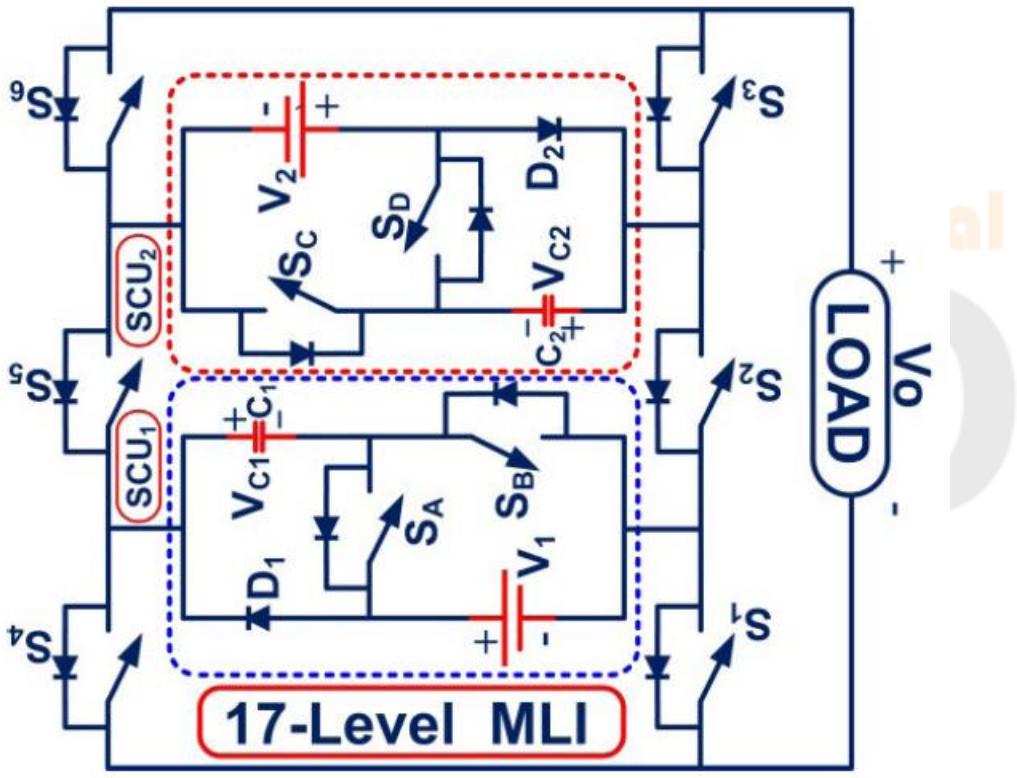
Figure 3.15 shows a short circuit possibility of each case.

IV PROPOSED ASYMMETRICAL 17-LEVEL MLI

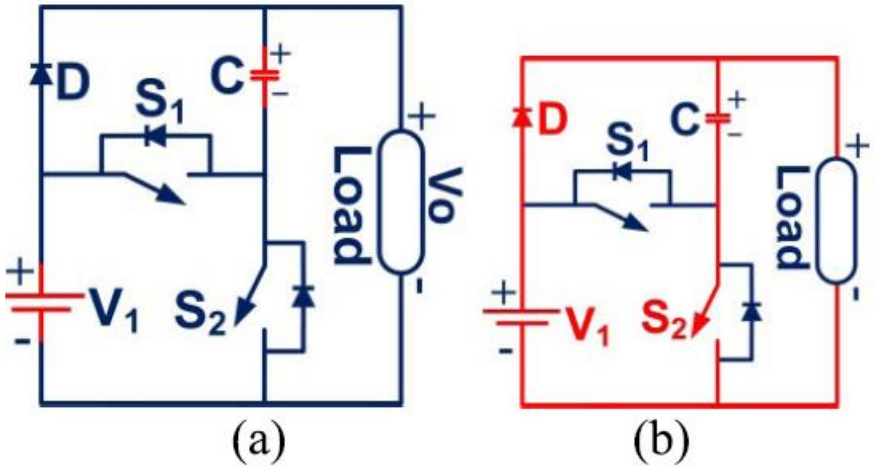
The proposed 53-level MLI is designed and implemented with a switched capacitor approach. SC is incorporated at the front end along with the H-bridge. It acts as an individual energy storage system for the proposed MLI. Hence it is essential to select the specific value of the capacitance, and the value depends on the operating frequency, load current

17-LEVEL MLI

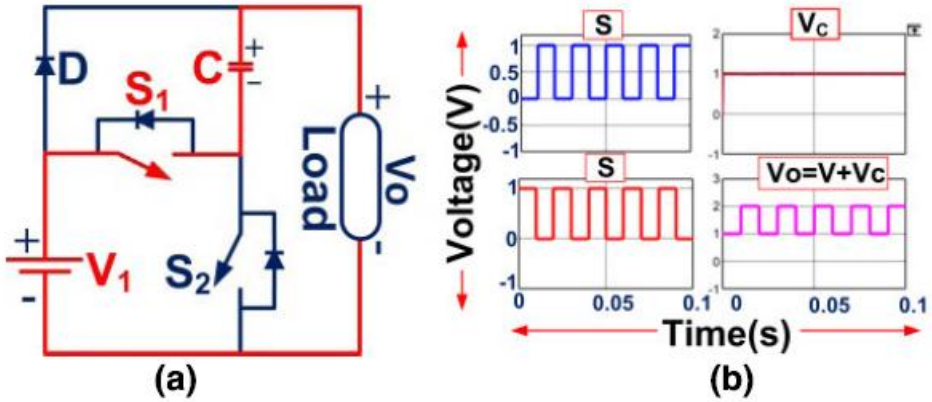
A 17-level MLI is designed with the two SC units connected in cascade with a smaller number of components is shown in FIGURE 9. The proposed MLI topology comprises 10 controlled switches with two asymmetric DC sources with the absence of inductors. The two DC sources are of unequal voltage levels formed to be an asymmetrical configuration. Several power quality issues like total standing voltage (TSV), cost factor, and cost per unit with various values of the weight factor, THD, switch count, component count level, voltage stress is minimized with this MLI topology. This topology achieves less TSV and is compared with various topologies. The path of the load current through the switches, along with the states of the operation is represented in TABLE III. Few modes of operation, along with the switching pulses, is shown in FIGURE 5, and the expected output waveform is represented



Developed structure of 17-level MLI.



SCU (a) Basic SC unit: (b) Charging.



Capacitor in SC unit: (a) Discharging, (b) Simulation output.

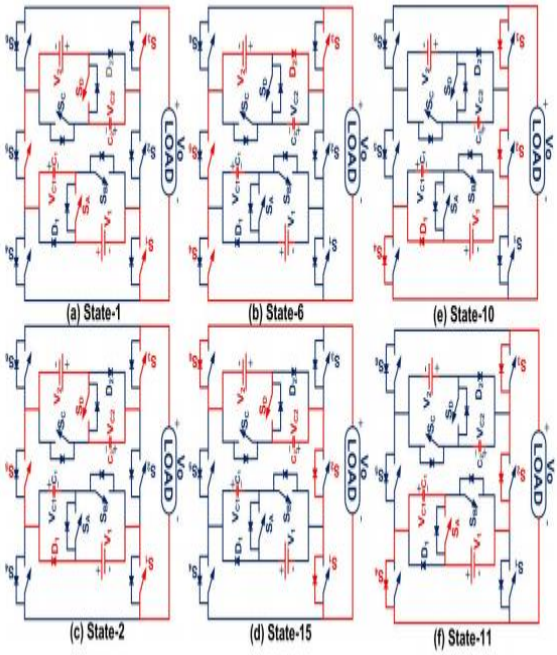
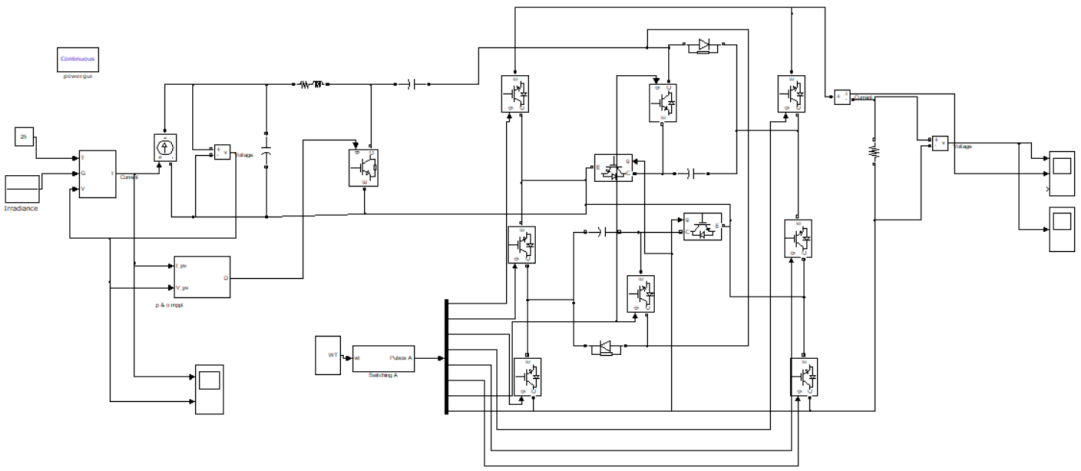
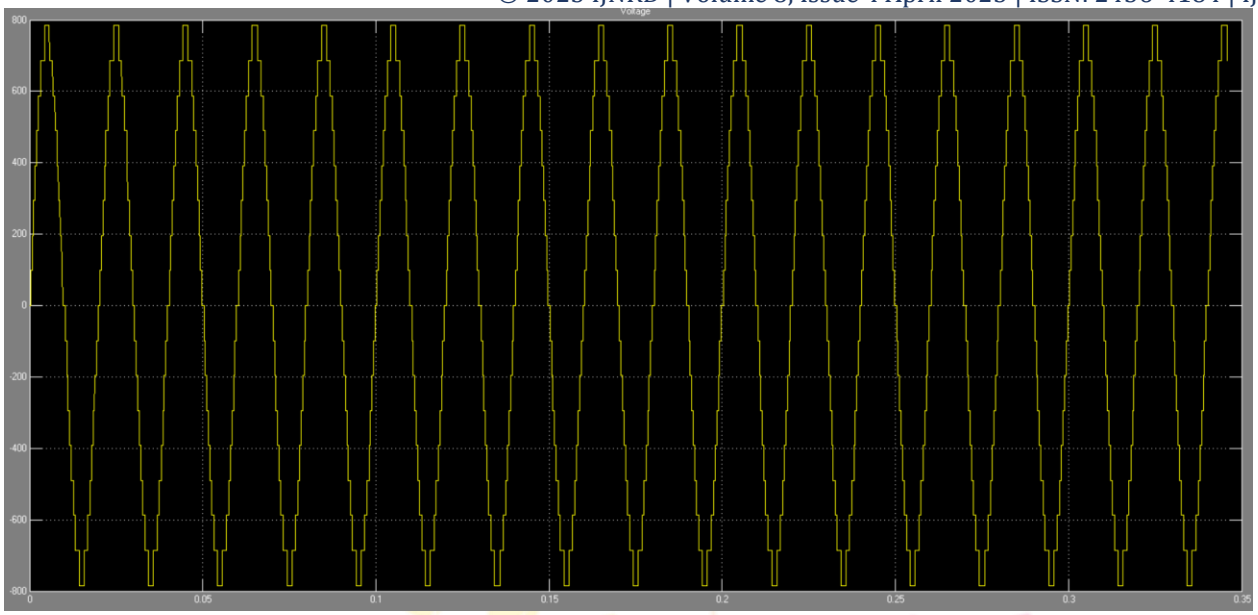


FIGURE 5. Modes of operation of the proposed 17-Level MLI topology.

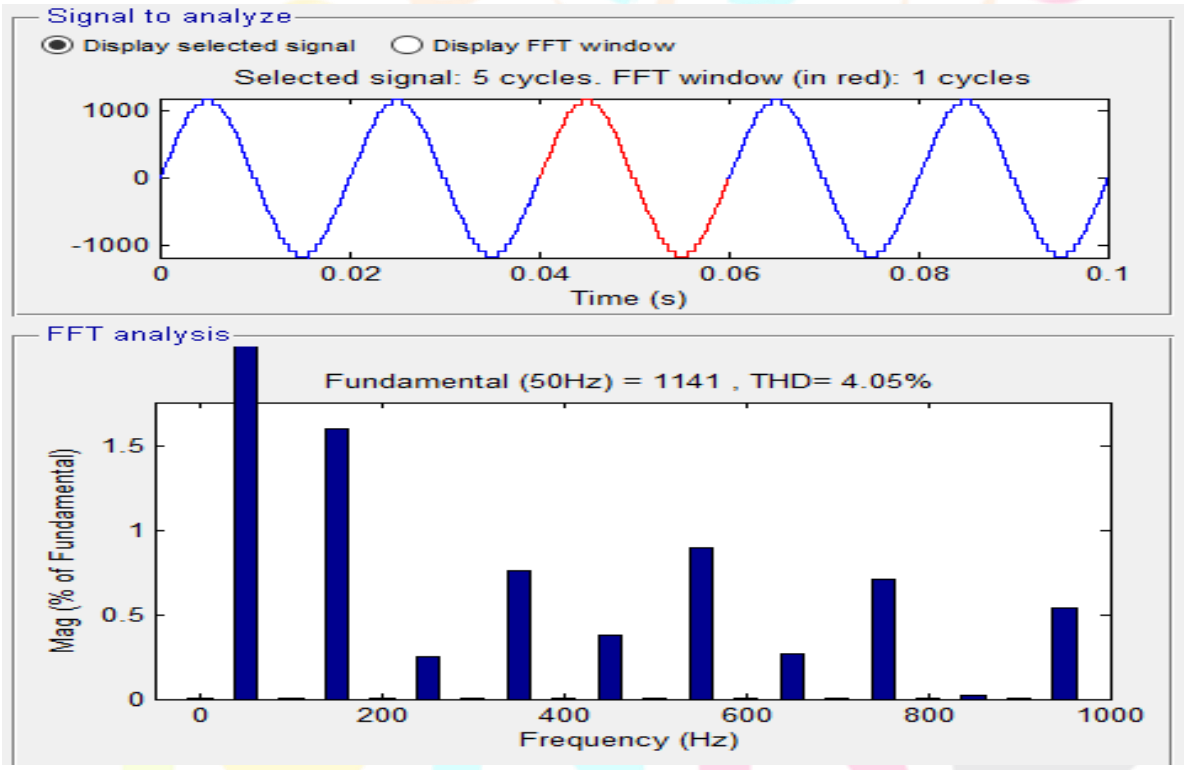
V.SIMULATION RESULTS



Circuit diagram



17 level Voltage waveform



Fft wave form THD 4.05%

VI.CONCLUSION

The proposed switched-capacitor based 53-level MLI topology for electric vehicle applications is designed and implemented for the solar PV energy system with lesser semiconductor devices to reduce the cost and size of the inverter, improving efficiency and reliability. P&O algorithm based MPPT technique is used, the stable output is achieved under all circumstances. The proposed MLI is implemented with various combinations of SC connections. A basic two units are cascaded and obtained a 17-level MLI configuration. The cascade connection of two 17-level MLIs results in the formation of a 33-level MLI, and the proposed 53-level MLI is achieved by cascading three SC

units. All the MLIs are designed and compared with various topologies based on several parameters like devices count, TSV, THD, and cost function per level count. The comparative analysis shows that the proposed MLI is more efficient with fewer power losses. It is noticed that both simulation and experimental THD are 1.41%. TSVpu is 1.15; efficiency is 94.21%, CF/L values for both values of α are 0.7 and 0.73, which clearly shows the cost is significantly less compared with various topologies. The proposed MLI is tested under multiple dynamic load variations. This topology is most suited for renewable energy applications.

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