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DESIGN AND COMPARITIVE ANALYSIS OF BINARY AND TERNARY SRAM CELLS

T. Venkata Lakshmi[1], G.G.V.S. Vardhan Kumar[2], A. Nandini[3], A. Dakshayini[4], Ch. Kavya[5]

[1]Associate Professor,[2345]Students

[12345]Dept of ECE, Seshadri Rao Gudlavalleru Engineering College, Gudlavalleru-521356, Andhra Pradesh, India

Abstract:

One of the biggest problems in portable applications, which are always in demand and include laptops, mobile phones, etc., is a low power circuit. Static Random Memory (SRAM) consumes a sizable portion of a system-on-a-chip (Soc) and considerably adds to the chip's overall power consumption, which is why efforts are made to develop low power Recurrently, there is a demand for the design of high performance and low-power memory circuits. Both high-performance processors and portable handheld devices require. SRAM as a key component.

With ternary inverters and inverters, we are creating SRAM. cells. The binary number system's fundamental unit is 2. (0,1). The base number for the ternary numeral system is 3. (0,1 and 2).

In the proposed project, binary and ternary SRAMs both from different cells will be compared, and performance traits such. propagation delay, power dissipation, as well as energy delay product will be monitored and determined.

Keywords:

Binary SRAMs, Ternary SRAMs, Power dissipation, Delay, Area, Average Power,

I. INTRODUCTION:

There is great potential for modern very large-scale integration (VLSI) circuit designs to be improved by multi valued logic (MVL) circuits [1]. Compared to binary systems, this system has a greater capacity for information storage. Ternary memory offers a higher store capacity than binary memory, which benefits from faster access times and lower costs.

In implantable devices and wireless applications where input power or battery life are major concerns, a low power Static Random Access Memory (SRAM) design is a major concern [1]. whose operating frequency ranges from a few hundred kilohertz to tens of megahertz [3] [2]. This is due to the System on Chips (SoC) SRAMs' significant contribution, which is reflected in their estimated occupancy of 70% of the die area (which may rise more in the future) [4]. These devices are now more power-hungry due to the growth of the transistor count in SRAMs and the accompanying leakage current of these transistors in the scaled-down technologies.

Low power Static Random Access Memory (SRAM) design is a critical challenge in implantable devices and wireless applications where input power or battery life are major concerns [1]. Its operational frequency spans tens of megahertz to a few hundred kilohertz [3] [2]. This is a result of the enormous contribution made by System on Chips (SoC) SRAMs, as evidenced by their estimated occupancy of 70% of the die area (which may increase more in the future) [4]. Because to the increase in the number of transistors in SRAMs and the resulting leakage current of these transistors in the downsized technologies, these devices are now more power-hungry.

II. LITERATURE SURVEY:

The purpose of this work is to examine the low power dissipation of 6T, 7T, 8T, and 10T SRAM cells during read operation with increase in transistor utilising 180nm technology. With the help of this study, we can reduce the additional transistor's power usage. In this study, we replace the system's DRAMs with a 6T SRAM manufactured in 45nm CMOS technology. We can get past the SRAM cell's substantial share of the total power. With

enhanced self-controlled voltage level circuits in 10T SRAM, we can deliver low leakage power here, resulting in total average power.

We can use less dynamic power and achieve excellent read stability by designing a low power 10T SRAM cell. Power consumption is lower, and stability is higher when compared to other technology. In this work, the average power dissipation is decreased using the adiabatic approach. Here, we can cut the power used for writing operations by 87%, hold operations by 66%, and read operations by 85%.

To compare the cells for read operation while minimising read and write access time and supply voltage, the goal of this research is to analyse the read behaviour of numerous SRAM cells in structures using cadence tools at 45nm technology. Examined are the leakage currents, leakage powers, and read behaviour of each SRAM cell. In contrast to the standard 6T SRAM cell as well as the 7T, 8T, and 9TSRAM cells, a 10T SRAM cell implementation is proposed here that results in decreased leakage power and leakage current as well as increased read stability.

III. PROPOSED SYSTEM:

Through performing a simulation of binary SRAM cells of sizes 6T, 7T, 8T, and 10T and putting into practise a design for basic Ternary Logic utilised in SRAM cells of those sizes, the proposed system outperformed the existing system. Ternary SRAM provides low power design for read and write operations, which is important for battery-operated portable devices. The key benefit of the ternary SRAM cell is reduced complexity of the interconnections may be achieved, which in turn reduces the chip space.

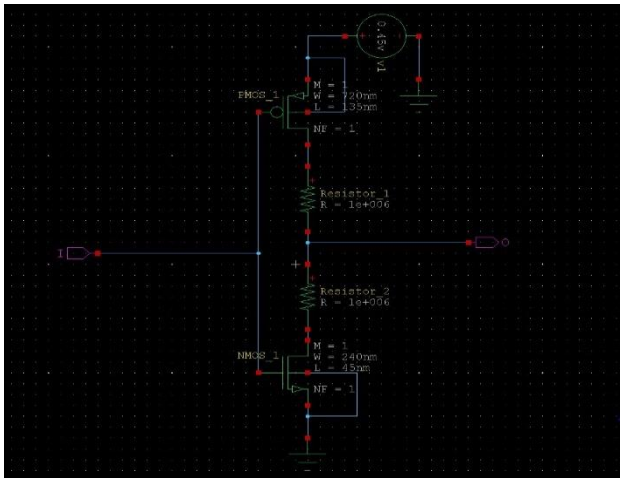
The project's main goal is to use binary and ternary logic to design binary SRAM and ternary SRAM cells. Additionally, contrast the various parameters of binary and ternary SRAM cells with different topologies.

IV. METHODOLOGY:

The project entails designing different binary and ternary SRAM cells as well as 6T, 7T, 8T, and 10T employing binary and ternary logic. Implementing different binary SRAM and ternary SRAM cells, doing functional verification, power, delay, and timing analysis with the Tanner tool, and comparing power and delay for binary and ternary SRAM cells.

4.1 Design of ternary inverter:

A ternary inverter requires three input states (0, 1, and 2) and one output state to function, making its design more complicated than a binary inverter's. The ternary inverter's input stage is made to work with three input levels, and the pull-up and pull-down networks amplify and invert the output of the device. The feedback loop controls how stable and oscillatory the inverter output is.



4.5 Design of Binary 6T SRAM cell:

According to Figure 1, the conventional cell has six transistors. Memory cells consist of two cross-coupled inverters and nMOS access transistors (A1 and A2) at the circuit's ends. Driver transistors for the latch's nMOS components are D1 and D2, while pull-up transistors for the latch's pMOS components are P1 and P2. When the word line is elevated, the access transistors activate and connect the cell to the bit lines for read or write operations.

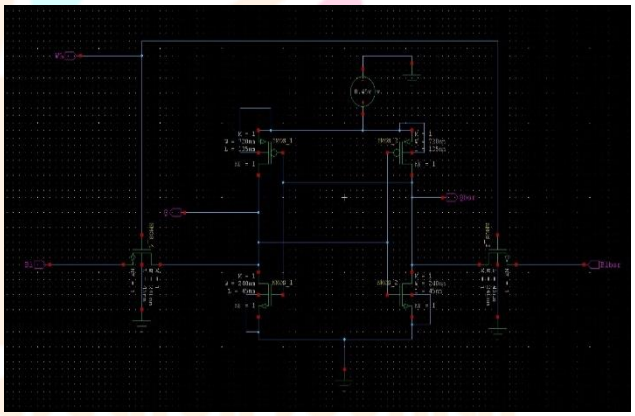


Fig 5: Binary 6T SRAM Cell

4.6 Design of Binary 8T SRAM cell:

In general, the suggested circuit's RSNM is at least 2.2X better than the conventional 6T-SRAM cell and is comparable to the standard 8T-SRAM cell given that the latter's write margin is not enhanced. The suggested cell has a single-ended read strategy, which unquestionably lowers the output swing.

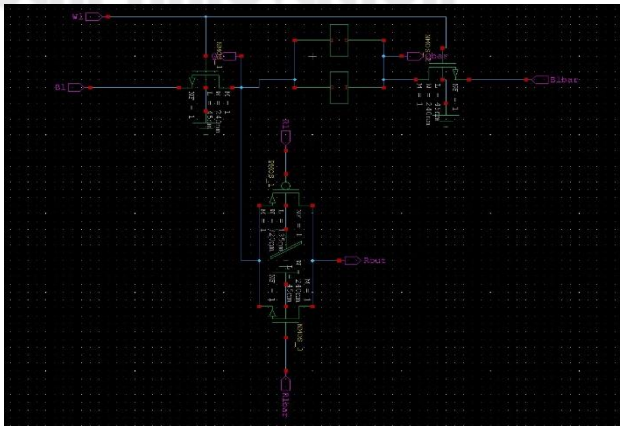


Fig 6: Binary 8T SRAM Cell

4.7 Design of Binary 10T SRAM cell:

The proposed 10T SRAM cell is seen in Figure 6. Three transistors are employed in the read route of the proposed 10T SRAM cell, adopting the stacking technique to increase the ION/IOFF ratio. Because read transistors do not share with other cells, there is no sneaky current in the read path. The integration of more SRAM cells sharing the same bit line is therefore made possible by having a higher ION/IOFF ratio. Because of the greater ION/IOFF ratio, SRAM peripheral for read and write of each column can be shared for an increasing number of cells. SRAM's enormous storing capacity allows for the saving of more space, energy, and money.

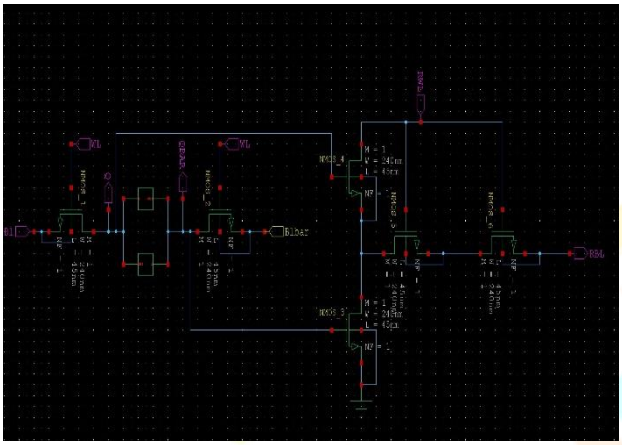


Fig 7: Binary 10T SRAM Cell

4.2 Design of ternary 6T SRAM cell

The structure comprises of two access transistors N3 and N4 that are utilized for read and write operations, as well as two cross-coupled CMOS inverters P1-N1 and P2-N2 that are used to store bits. In read mode, the SRAM cell's 0 or 1 stored value is extracted. The word line is turned on, which turns on the N3 and N4 access transistors. The sensing amplifier detects the voltage drop in the BL or BLB. The value of "q" is determined with the use of a sense amplifier.

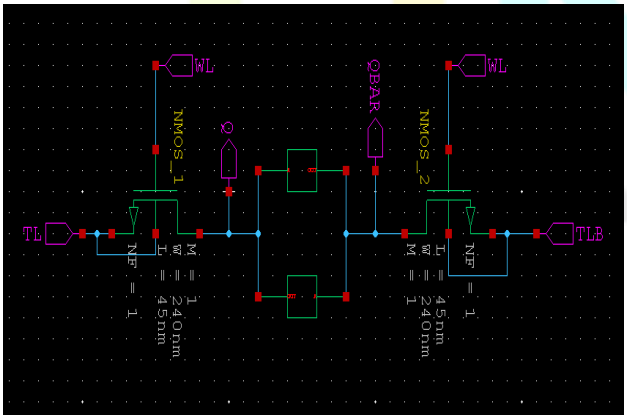


Fig 2: Ternary 6T SRAM Cell

4.3 Design of ternary 10T SRAM cell:

The schematic representation of projected 10T SRAM circuit is depicted in Figure 2Figures 1 and 3 show, respectively, active, and inactive devices during read and write operations of the suggested topology. Upon being read, the suggested topology operates in differential mode, as seen in Figure 1b. For the suggested architecture, transistors P1 and P2 constitute the core latch structure, along with transistors N1 and N2. Read (RD) and write (WR) signals, correspondingly, control the gate of access transistors N3 and N4.

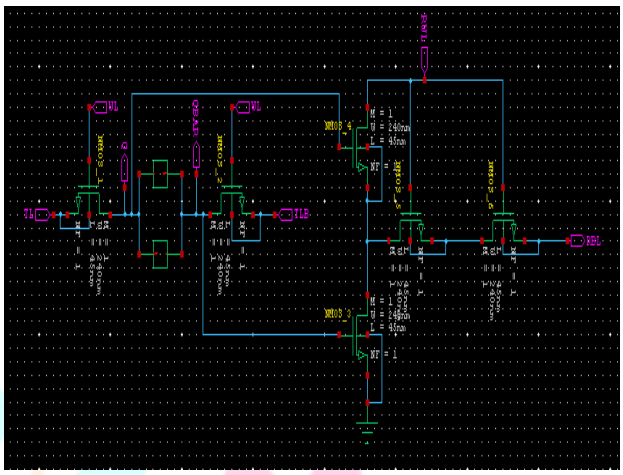


Fig 3: Ternary 10T SRAM Cell

4.4 Design of ternary 8T SRAM cell:

The 8T-SRAM cell that has been proposed adds two transistors—one NMOS and one PMOS—to the conventional 6T-SRAM cell while keeping the read mechanism single-ended. Just the RWL signal is asserted during read, whereas the WWL and RWL signals are both set to high during write. When a "1" is stored on the storage node Q in this SRAM cell configuration, transistor PUC is used to increase the write margin of the circuit. When QB is set to "0" in this mode, the voltage on NF's drain rises, which reduces PUC's ability to be driven.

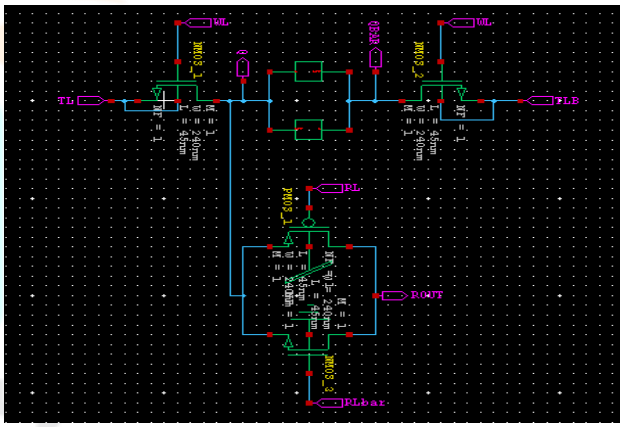


Fig 4: Ternary 8T SRAM Cell

V. EXPERIMENTAL RESULTS:

The proposed architecture is compared for the read operation alone because it can do both the read and write operations. Thus, the read and write states are considered in the results given here. SRAM performance analysis often bases its conclusions on variables like power consumption, delay, and power delay product (PDP).

5.1 Binary SRAM Cell:

	Techno-logy	Power Supply	Avg. Power (uW)	Delay (ns)	PDP (zJ)
6T	45nm	0.45v	0.1066	10.002	1.060
10T	45nm	0.45v	0.112	9.912	1.110
8T	45nm	0.45v	0.09	9.890	0.890

5.2 Ternary SRAM Cell:

	Technology	Power Supply (mV)	Avg. Power (uW)	Delay (Ns)	PDP (zJ)
6T	45nm	450	0.125	0.723	0.090
10T	45nm	450	0.119	6.156	0.732
8T	45nm	450	0.1044	0.456	0.047

VI. CONCLUSION:

Static random-access memory (SRAM) cells come in binary, ternary, and other configurations. A larger memory density is possible with ternary SRAM cells as opposed to binary SRAM cells since they may store data in three different states.

Because of its simplicity, high speed operation, and low power consumption, binary SRAM cells are widely employed. They are made up of two cross-coupled inverters formed by six transistors, each of which can store one bit of data. Because of its excellent performance and low power requirements, binary SRAM cells are frequently employed in computer memory systems.

On the other hand, ternary SRAM cells can store data in three states: 0, 1, and 2. Compared to binary SRAM cells, this enables larger memory densities because each cell can store several bits of data. Ternary SRAM cells operate slower and consume more power than binary SRAM cells because storing and reading data in three states requires more intricate circuitry and transistors.

In conclusion, because to their great performance and low power consumption, binary SRAM cells are more straightforward and frequently employed. More memory density is provided by ternary SRAM cells, albeit at the cost of more complicated circuitry and power usage. According on the needs of the application, such as memory density, power consumption, and operating speed, one must decide which SRAM cell to utilise.

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