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Ultra-Low Power Approximate Multipliers Using Energy Recovery Logic

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ABSTRACT

Multipliers are crucial components in digital signal processors, especially in applications like multimedia, machine learning, and data mining. In such applications, approximate circuits can be used to reduce area, power, and delay while still maintaining acceptable levels of accuracy. Adiabatic logic is a low-power technique that can be employed to further reduce power consumption. In this study, approximate 4-bit array multipliers were designed using both traditional CMOS and PFAL adiabatic logic, and then implemented in Cadence virtuoso. The results showed that the PFAL circuits achieved power savings of approximately 59% compared to CMOS logic. This highlights the potential of PFAL circuits for battery-operated portable systems where power consumption is a critical concern.

Keywords: Approximate computing, adiabatic logic, CMOS, Positive feedback adiabatic logic, power dissipation.

INTRODUCTION

In today's digital world, the demand for high-speed and low-power electronic devices has increased significantly. One of the critical components of modern digital circuits is the multiplier. Multipliers are used in a wide range of applications such as signal processing,

cryptography, and image processing. The performance of these applications largely depends on the speed and accuracy of the multiplier used. However, the conventional multiplier architectures consume a significant amount of power and dissipate heat, which is a major concern for portable and low-power applications [1].

Researchers have been investigating several design methodologies to create energy-efficient multipliers to address this issue. One such technique is the use of adiabatic logic, which has gained considerable attention in recent years due to its potential to reduce power consumption.

Adiabatic logic is a design method that makes use of the idea of energy recycling to cut down on power usage. In adiabatic logic, the energy stored in a circuit element is recycled back into the circuit instead of being dissipated as heat. This approach can significantly reduce power consumption and can be particularly effective for applications where power dissipation is a major concern [2-3].

Adiabatic logic can be utilized to create energy-efficient multiplier architectures that run at high speeds and with little power usage in the context of approximate multipliers [4]. One of the key advantages of adiabatic multipliers is that they can be designed to operate on a reduced set of logic gates, which can significantly reduce power consumption and improve the overall efficiency of the system.

There are several types of adiabatic multipliers, including charge recovery multipliers, switched capacitor multipliers, and resonant clocked multipliers. Each of these designs has its advantages and disadvantages and can be optimized for specific applications.

Inconclusion, energy-efficient approximate multipliers using adiabatic logic are an exciting development in the field of digital circuit design. These designs can

significantly reduce power consumption while maintaining high-speed performance, making them ideal for portable and low-power applications. With ongoing research and development in this area, we can expect to see more efficient and effective adiabatic multiplier architectures in the future.

LITERATURE REVIEW

S. K. Aggarwal and R. K. Nagaria proposed a design of an adiabatic approximate multiplier with improved performance in 2016. This paper presents a design of an adiabatic approximate multiplier that uses a modified 4-2 compressor. Compared to current approximation multipliers, the suggested multiplier enhances performance while consuming less power.The simulation results show that the proposed multiplier has better energy efficiency and lower power consumption [5].

M. A. Sedaghat and M. A. Pourmina proposed a design of a low-power approximate multiplier using adiabatic logic in 2016. This paper presents a new approach for designing a low-power approximate multiplier using adiabatic logic. The proposed multiplier is based on a modified carry-save adder and uses adiabatic logic to reduce power consumption. The simulation results show that the proposed multiplier has better energy efficiency and lower power consumption compared to existing approximate multipliers [6].

S.S. Sathya and S. P. Siva Prasad designed an adiabatic approximate multiplier design using hybrid logic in 2017. This paper proposes a design of an adiabatic approximate multiplier using a hybrid logic style that combines complementary metal-oxide-semiconductor logic and adiabatic logic. The proposed multiplier uses a 4-2 compressor and reduces power consumption while maintaining high accuracy. The simulation results show that the proposed multiplier has better energy efficiency compared to existing approximate multipliers [7].

M. Sharma and S. P. Siva prasad proposed a design of a low-power adiabatic approximate multiplier using the MTCMOS technique in 2019. This paper presents a design of a low-power adiabatic approximate multiplier using MTCMOS technique. The proposed multiplier reduces power consumption and improves energy efficiency while maintaining high accuracy. The simulation results show that the proposed multiplier has better energy efficiency compared to existing approximate multipliers [8].

BACKGROUND

Array Multiplier

An array multiplier is a digital circuit that performs the multiplication of two binary numbers. It is a type of combinational circuit that uses an array of full adders to perform the multiplication.

The basic idea behind an array multiplier is to break down the multiplication into a series of smaller, simpler operations. Each multiplier bit is used to choose a portion of the final product, which is created by moving the multiplicand by the corresponding bit position.The partial products are then added together using a series of full adders [9].

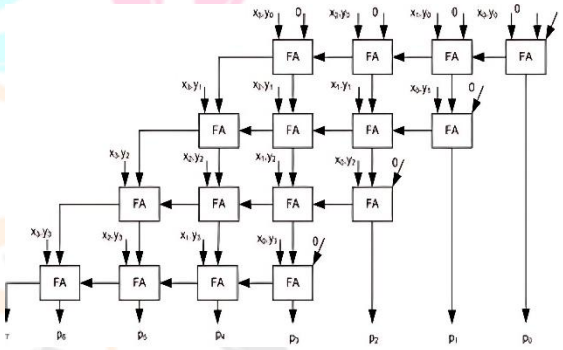
For example, consider the multiplication of the binary numbers 1011 and 1101:

1 0 1 1 (partial product, shifted 1 bit)

0 0 0 0 0 (partial product, shifted 2 bits)

1 0 1 1 (partial product, shifted 3 bits)

1 1 1 0 0 1 1 (product)



In this example, each bit of the multiplier selects a partial product, which is generated by shifting the multiplicand by the corresponding bit position. The final product is then created by adding the partial products together using a succession of full adders.

Array multipliers are commonly used in digital signal processing (DSP) applications such as image and audio processing, where large numbers of multiplications need to be performed in real-time. They are also used in computer arithmetic units to perform integer and floating-point multiplication.

The multiplication of two unsigned 4-bit numbers (X and Y) can be done using an add-and-shift algorithm from Fig. 1. In order to do this, multiply the multiplicand by each bit of the multiplier to produce partial products. The partial products are then arranged according to their bit position and added together to get the sum bits of the result.

From Fig. 2 The 4-bit array multiplier shown in the block diagram produces the partial products using a conventional topology made up of two inputs AND gates. Each row of partial products is shifted according to the bit position of the multiplier, forming a partial-product array. The array multiplier can be expanded to handle wider bit widths and is an effective method for performing binary multiplication. This process can be

visualized as a grid like structure, where each row represents a partial product and each column represents a bit position in the final result. The array multiplier is an efficient way to perform binary multiplication and can be extended to larger bit widths as well.

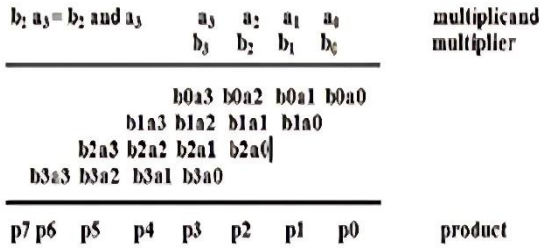


Fig. 1: 4-bit array multiplication algorithm

Fig. 1: Block Diagram4-bit array multiplier

Static implementation

CMOS is a widely used technology for designing digital circuits. In CMOS, logic gates are implemented using pairs of MOSFETs, where one acts as a pull-up transistor (p-type) and the other acts as a pull-down transistor (n-type).

Fig. 3 is CMOS implementation of full adder that adds three binary numbers: A, B, and a carry-in (Ci), and produces a sum (S), and a carry-out (Co). Two half adders and an additional OR gate to provide the carry-out bit can be used to implement a complete adder.

Fig. 4 shows the static implementation of half adder. To create the sum and the carry-out bit, a half adder can be built using two XOR gates and an AND gate, respectively.

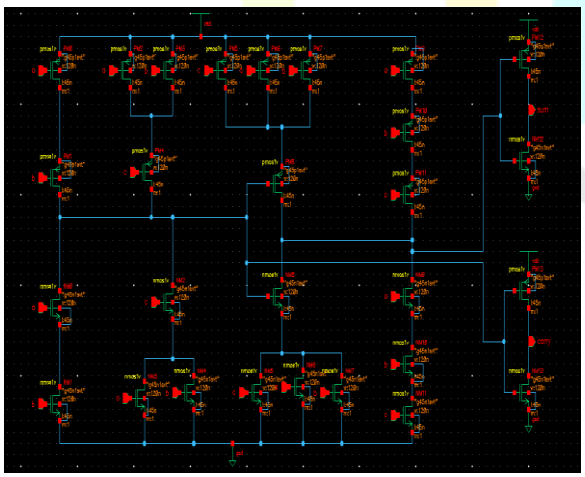


Fig. 3: Full adder Using CMOS

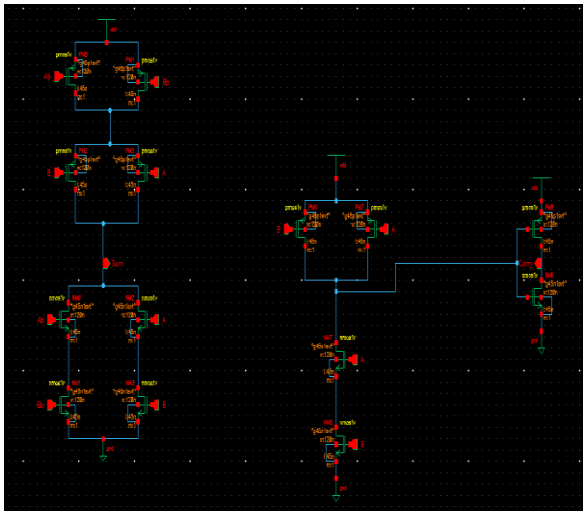


Fig. 4: Half adder Using CMOS

Approximate Multipliers:

To reduce power consumption in approximate multiplication, one technique is the partial product perforation method. This involves skipping the generation of some partial products when multiplying two n-bit numbers, X and Y. By doing so, the accumulation of operands is reduced, which can eliminate n full adders from the accumulation tree. The final result of X × Y is obtained by summing the remaining partial products Xyi, where yi is the ith bit of Y.

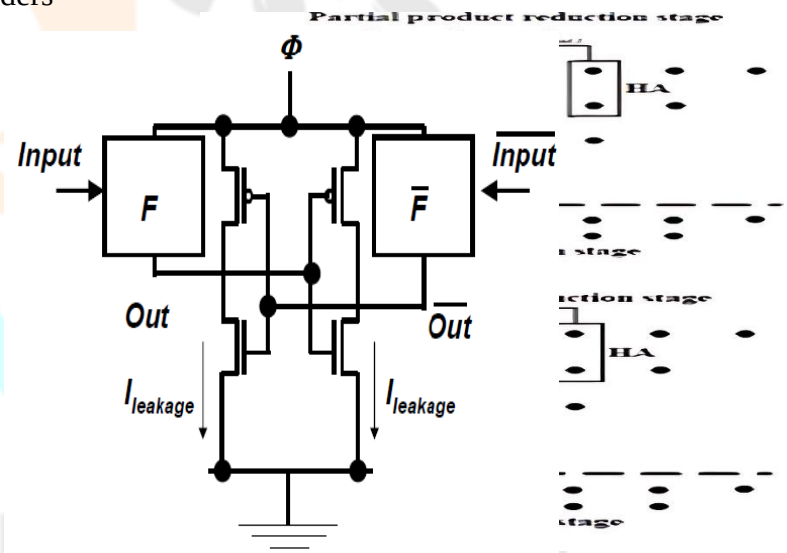


Fig. 5: 4-bit partial product reduction

Adiabatic logic:

Positive Feedback Adiabatic Logic (PFAL) is a type of logic family that is designed to minimize power consumption by reducing the energy dissipation in the charging and discharging of the parasitic capacitances associated with digital circuits. PFAL achieves this by using positive feedback to latch the state of the output,

which reduces the number of transitions and thus the power consumption [10].

From Fig. 6 the output node of a gate is connected to the input through a pair of complementary transistors, which form a latch. The latch is activated by a pulse signal that triggers the complementary transistors to conduct, allowing the output to change state. Once the output has settled, the latch is deactivated, and the complementary transistors are turned off, resulting in very low power dissipation.

The pulse signal that triggers the latch is typically generated using adiabatic charging and discharging techniques, which help to minimize energy dissipation by controlling the charging and discharging rates of the parasitic capacitances. Energy is transferred to and from the parasitic capacitances using carefully timed signals in adiabatic charging and discharging methods, which reduce energy losses from heat dissipation.

Fig. 6: Basic PFAL structure

The design of a Half Adder and Full Adder using Positive Feedback Adiabatic Logic (PFAL) involves using complementary transistors in a positive feedback loop to latch the output state and reduce power consumption**.**

Fig. 7 and Fig. 8 respectively show the half adder and full adder circuits using PFAL logic.

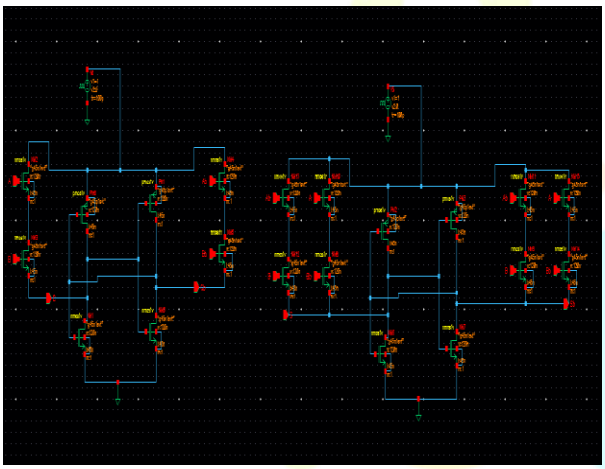


Fig. 7: Full adder Using PFAL

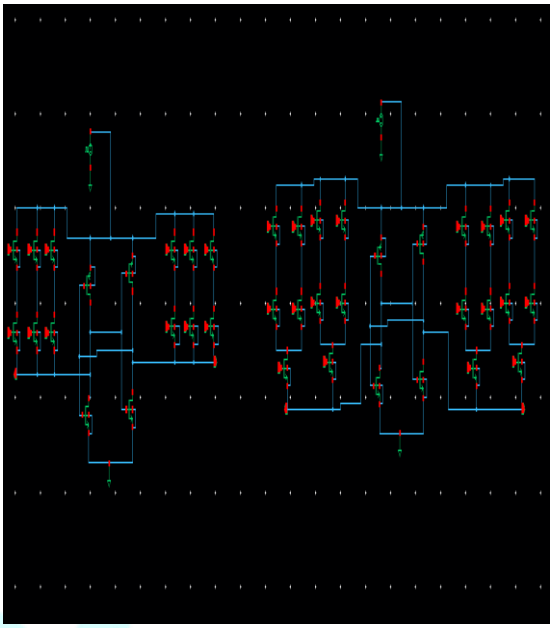


Fig. 8: Half adder using PFAL

PERFORMANCE EVALUATION OF APPROXIMATE MULTIPLIERS:

The goal of the study was to compare the power consumption and performance of CMOS and PFAL adiabatic logic-based approximate multipliers. To achieve this 4-bit approximate multipliers were designed using both types of logic and then implemented in cadence. The design schematics for approximate array multipliers are shown in Fig. 9 and Fig. 10 respectively show the approximate Multiplier using both CMOS and PFAL.

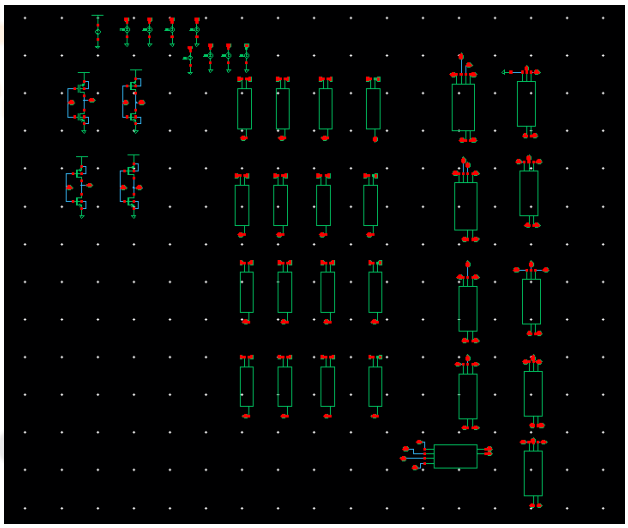


Fig. 9: Approximate multiplier using CMOS

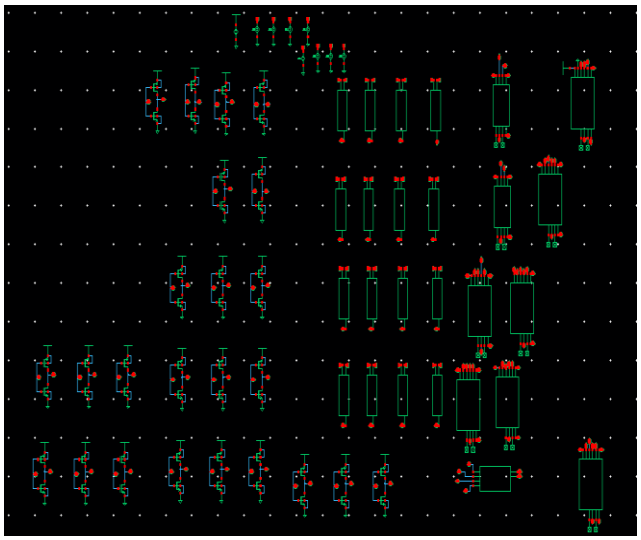


Fig. 10: Approximate multiplier using PFAL

The study conducted power analysis for both CMOS and PFAL-based approximate 4-bit multipliers, and the results are presented in Table 1. The analysis showed that for approximate multipliers, the power consumption in the PFAL circuits was significantly lower compared to the CMOS circuits. Therefore, PFAL logic is a more power-efficient option and suitable for designing energy-efficient systems.

Table 1: Comparison of power dissipation of 4-bit approximate multiplier circuit using CMOS and PFAL logic

Supply voltage (V)	Average Power Dissipation (nW)	
	CMOS	PFAL
0.8	82.76	45.09
1	84.63	45.11
1.2	85.0	45.14

CONCLUSION:

The project involves designing 4-bit multipliers using both CMOS and PFAL adiabatic logic, followed by simulation using the Cadence tool to verify functionality. Power analysis is performed, and the power consumption is calculated and it is compared to approximate multipliers using CMOS and PFAL circuits. The results indicate that adiabatic logic is the most suitable approach for developing energy efficient portable systems.

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