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Design of 16-bit Adder, Multiplier and ALU using Reversible Logic Gates

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ABSTRACT: Increasing demand for reduction in power dissipation in digital computer system has led to new mode of computation for digital design giving birth to reversible computing. Its main objective is low power dissipation in logical elements but can have some other advantages like error prevention and data security. In present-day, reversible logic has bring out to be an optimistic computing model having applications in low power CMOS, nanotechnology, quantum computing and DNA computing. This paper presents about various purposed schemes used to design a 16-bit Adder, 16×16 Multiplier and Arithmetic & Logical Unit using Reversible Logic Gates. The reversible Adders, Multipliers and ALUs are optimized in terms of total quantum cost, number of ancillary inputs, number of garbage outputs and hardware complexity.

Keywords— *Adder, Multiplier, Arithmetic and Logic unit (ALU), power dissipation, application specific reversibility.*

1. INTRODUCTION

One of the most interested topics in current researches of hardware designers is the low power circuit design. The one of the main concern in VLSI design is power dissipation. According to Moore's Law statement that the number of components on the chip will double for every 18 months. After studying the Moore's Law researchers have come to decide that as the number of components on the chip increases the power dissipation will also increases. In past different techniques were used to reduce power dissipation hence for VLSI designers the power minimization has become a prime factor. In recent times the one of the alternative technique to reduce power dissipation is reversible logic.

The Primary objective of a digital circuit design is to optimize for speed, area, power and energy. While it's a challenge for circuit designers, to achieve this optimization without compensating for one or theother parameters mentioned above. Certain design techniques, algorithms and smarter planning of the available resources have proven to be successful to achieve the level of optimization required for much higher efficiency. Adder, Multiplier and Arithmetic Logic Unit (ALU) being the driving components of a processor, optimizing its module for speed and power becomes quite inevitable. Many previously published

technical papers have emphasized the use of reversibility in circuits design for reduction in power dissipation,[4] while successfully demonstrating the same. However, this reduction in power was also followed by significant reduction in speed as well as increase in chip area. Hence smarter algorithm and logic design was required to speed up the execution of a logic module.

2. REVERSIBILITY:

The strengths of Reversibility in digital circuits is well documented and explained in article [1]. A circuit which can undo or reverse its outputto get back its original input will not suffer information loss, since all the information are present within the circuit and only need to be reversed, to be recovered. Hence a reversible circuit will save major chunk of power dissipation suffered due to information loss that happens every clockcycle.

The basic requirement of a reversible circuit is to have a one-to-one correspondence between inputs and outputs, which requires the input and output pin count to be same. Also each input state must correspond to a particular unique state of the output i.e. output states cannot be shared by more than one input states available. If the above criteria are satisfied the inverse circuit can be easily designed to make the circuit reversible.

2.1 Reversible Gates

A reversible logic gate is an n-input, n-output device with one-to-one mapping, which helps to retrieve the inputs from the outputs and vice-versa. The main challenges for the reversible logic [3] are reducing the power dissipation, reducing number of gates, delay and quantum cost.

The reversible gates used in this paper are as follows.

Peres Gate

Peres gate is a 3x3 reversible gate as shown in Fig 1. The quantum cost of this gate is 4. It is mainly used for half adder application. It has lesser area and quantum cost compared to other reversible gates like Fredkin and Feynman gate. It has three inputs A, B and C. The outputs are given as P=A,Q=A xor B and R=(A.B) xor C. To use it as an half-adder C is given logical zero. The outputs of the gate become P=A, Q=A xor B and R=A.B.

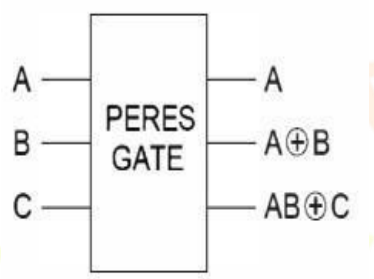


Fig 1: Peres Gate

HNG Gate

HNG gate is a 4x4 reversible gate as shown in Fig 2. It is mainly used for full adder application. The quantum cost of this gate is 6. It has four inputs A, B, C and D. The outputs are given as P=A, Q=B, R=A xor B xor C and S= (A xor B).C xor (AB xor D). To use it as a full adder D is assigned to logical zero and C is assigned the input carry bit. The outputs of the gate become P=A, Q=B, R= A B C and S= (A xor B).C xor AB.

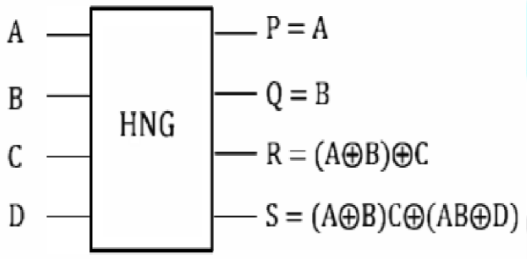


Fig 2: HNG Gate

BJN Gate

It is a 3x3 reversible gate as shown in Fig 3. The quantum cost of this gate is 5. For the three inputs A, B and C the outputs are P=A,Q=A and R=(A+B) xor C. In this paper it is used in the logical unit. This gate is used to realize OR and NOR gates. When C=O, R= (A+B) and for C=l, R= (A+B).

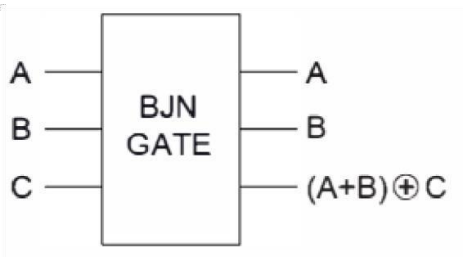


Fig 3: BJN Gate

TSG Gate

It is a 4x4 reversible gate as shown in Fig 4. This gate can realize most of the Boolean logical operations like AND, NAND, XOR, XNOR and NOT. The outputs of this gate are P=A, Q=A'C' xor B', R= (A'C' xor B') xor D and S= (A'C'xorB') D xor (AB xor C). Inputs C and D are used as control signals to select the logicaloperation.

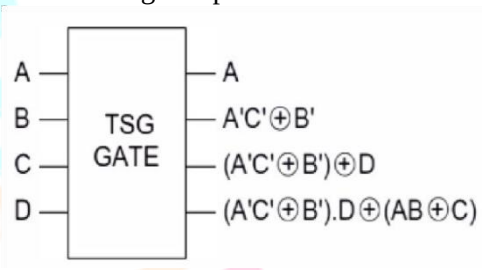


Fig 4: TSG Gate

2.2. 16-Bit Reversible Adder

The basic building block of the ripple carry adder is full adder. The binary full adder adds each input along with the applied carry in that is obtained as carry out from the addition of previous lower bits. To add two n bit binary numbers [5] then n binary full adders should be interconnected.

A Ripple carry adder is the inter connection of full adders. The general output expressions for a ripple adder are

$Si = A \oplus B \oplus Ci$

$Ci+1 = (A \oplus B) .Ci \oplus AB$ (i=0, 1, 2, 3, 4……)

The 16 bit adder is obtained by cascading the 16 full adders in series. The block diagram of four bit ripple carry adder using Peres gate is shown in Fig 5 below

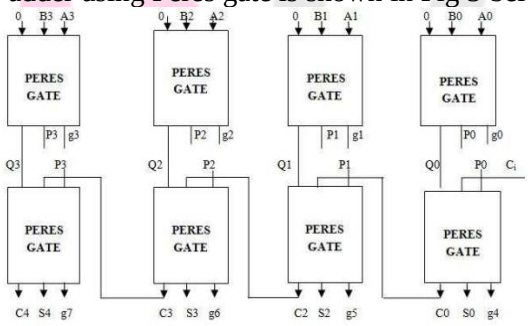


Fig 5: 16-bit adder using peres gates.

16-bit adder using peres reversible gates has been modeled in Verilog HDL and module structure is as shown in Fig-6

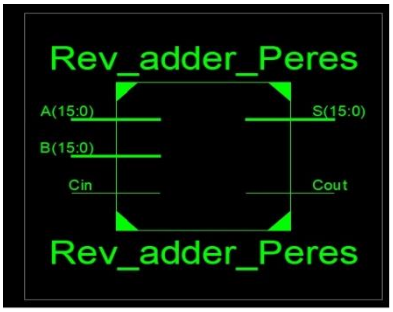


Fig 6: module structure of 16-bit adder.

2.3. 16-Bit Reversible Multiplier

Reversible multiplier is a digital circuit, used to multiply two or more binary numbers. Multiplication is used as arithmetic operations in many computational units. It is necessary for a processor to have high speed multiplier as described in [2]. So, now a day reversible multipliers are in demand. The basic cell for multiplier is a full adder. The multiplier design has two segments which work sequentially:

Segment 1: Partial Product generation

Segment 2: Addition of Partial Products generated in the segment 1.

We have presented a 16-bit multiplier as shown in Fig 7 modeled using Verilog HDL such that it has 16-bit multiplicand and 16-bit multiplier as inputs and produces a 32-bit result as product.

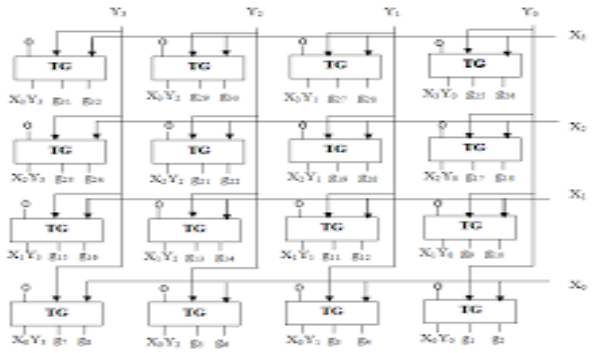


Fig 7: 16x16 multiplier using reversible gates

16-bit multiplier using reversible gates has been modeled in Verilog HDL and module structure is as shown in Fig-8

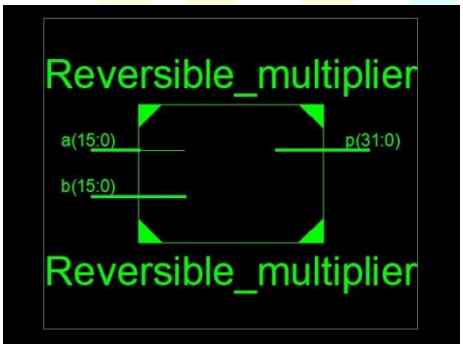


Fig 8: module structure of 16x16 multiplier.

2.4. Arithmetic Unit- Full-Adder/Subtractor

This adder is a 4-bit ripple carry adder.It is made using four HNG gates. HNG gates have the minimum delay, area and quantum cost for full adder application. The two inputs and carry bit is given to the first, second and third input respectively of the HNG gate. The fourth input pin of this HNG gate is grounded so it acts as a full adder. The output bits of the HNG will be P=A, Q=B, R = (A xor B) xor C, S = (A xor B).C xor AB. R is the sum of the addition and S is the carry. A control signal S is used to switch between adder and subtractor mode. When S=0, the circuit acts as a 4-bit full adder. When S=1, input b is complemented and an input high carry bit is given to the LSB full-adder. In subtractor, R is the difference and S is the borrow bit. If the result of the 4-bit subtraction is negative then the borrow will be zero and output is stored as 2'scomplement.

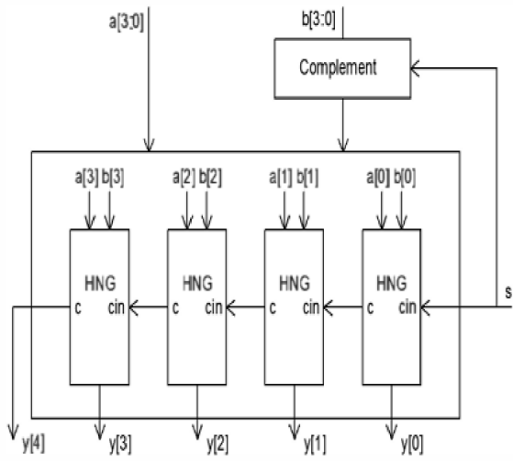


Fig 9: Reversible Full Adder/Subtractor

Proposed KSA Gate:

It is a 4x7semi-reversiblelogicgatedesignedespecially for 2-bit multiplication application. Out of the seven outputs, the first four outputs give the product of the two 2-bit inputs assigned to the four input pins. Three more output pins are added to make one-to-one mapping between inputs and outputs. Since this gate has 7 output bits it is expected to have one-to one mapping between all the128 cases. The proposed semi-reversible gate as shown in Fig10 has one-to-one mapping between the inputs and outputs for the possible 16 cases of output product. Using a general purpose reversible gate for a specific application has more number of redundant gates and garbage outputs.

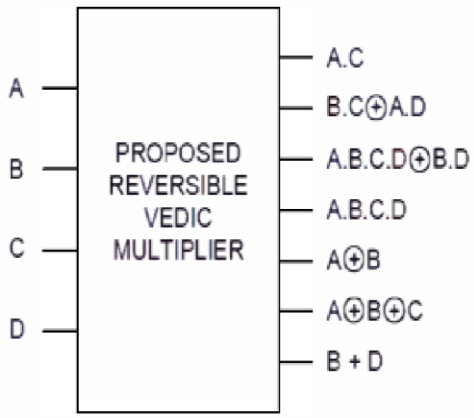


Fig 10: TSG Gate Proposed KSA Gate

2.5. Logical Unit

The proposed 4-bit logic unit performs the logic

operations on two 4-bit numbers. The 8 basic logic operations performed by proposed logic unit are AND, NOR, XNOR, XOR, NOT (invert), NAND, A'B, OR, NOR etc. A BJN gate is used to implement OR and NOR operations.

A control input C controls the operation of a BJN gate. When C=O, BJN gate performs OR operation of two inputs A and B. When C=l, it gives NOR operation of A and B. TSG gate is used to implement the rest of the logical operations. Input C and D acts as control signals to TSG gate. When c=0 and D=0, it results in AND operation of A and B. When c=0 and D=l, it gives XOR and XNOR operations of A and B. When C=1and d=0, the resulting output is inversion of B and NAND operation of A and B. When C=1and d=1, it results in A'B. Thus, overall logic unit uses only two types of reversible gates to implement 8 logic operations.

2.6. ALUDesign

The proposed ALU design[6] has a four bit control signal as shown in Fig 11.

- It performs six arithmetic operations andseven logical operations.
- The proposed ALU uses both reversible and semi reversible gates init.

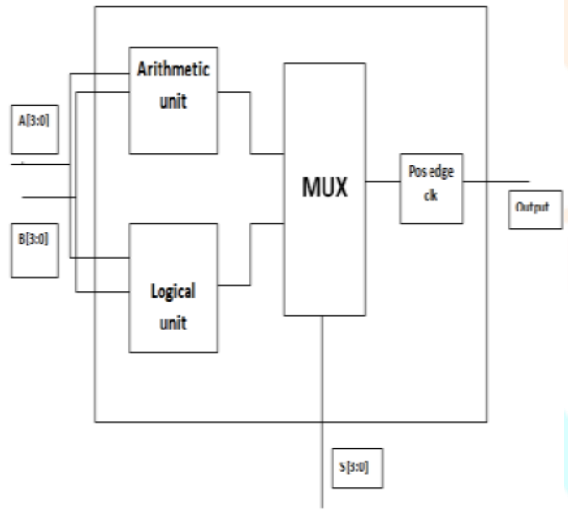


Fig 11: Proposed Architecture of ALU

The operations performed based on the control bits are as follows. Total of sixteen operations are performed by the proposed ALU as given in the below Table-1.

Table 1. Operations performed based on the control signal

Control Signal	Operation
0000	Addition
0001	Subtraction
0010	Multiplication
0011	Increment
0100	Decrement
0101	A.B
0110	A⊙B
0111	$\overline{A \odot B}$
1000	$\overline{B}$
1001	$\overline{A.B}$
1010	$\overline{A}.B$
1011	A+B
1100	$\overline{A+B}$

3. SIMULATION RESULTS

3.1 Simulation Result of 16-bit adder:

Below figure Fig-12 represents the simulation results of 16-bit adder designed using Peres reversible gates through Xilinx ISE 14.2v tool.

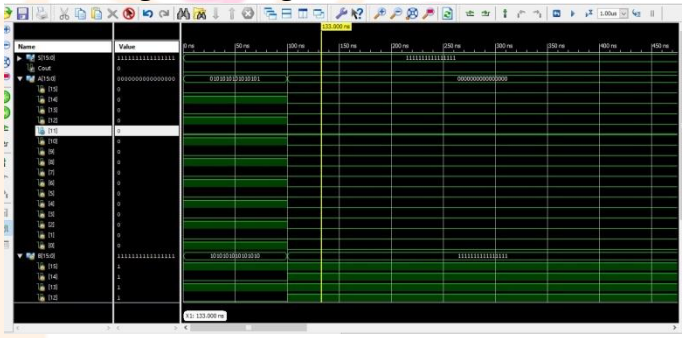


Fig 12: Addition of two 16-bit binary numbers

3.2 Simulation Result of 16x16 multiplier:

Below figure Fig 13 represents the simulation results of 16x16 multiplier designed using reversible gates through Xilinx ISE 14.2v tool.

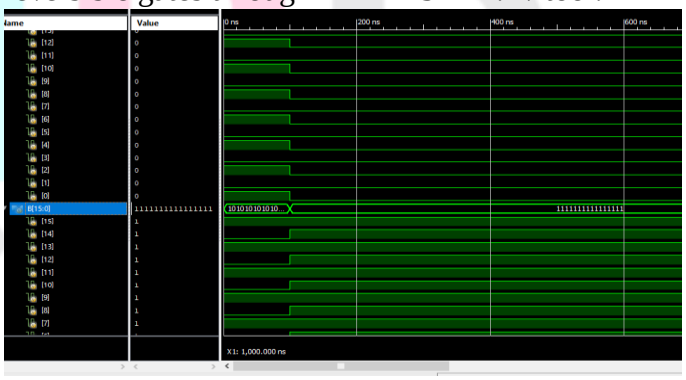


Fig 13: Multiplication of 16x16 binary numbers

3.3 Simulation Result of ALU:

Below figures Fig 14, Fig 15, Fig 16 represents the simulation results indicating some of the operations performed using reversible gates in ALU.

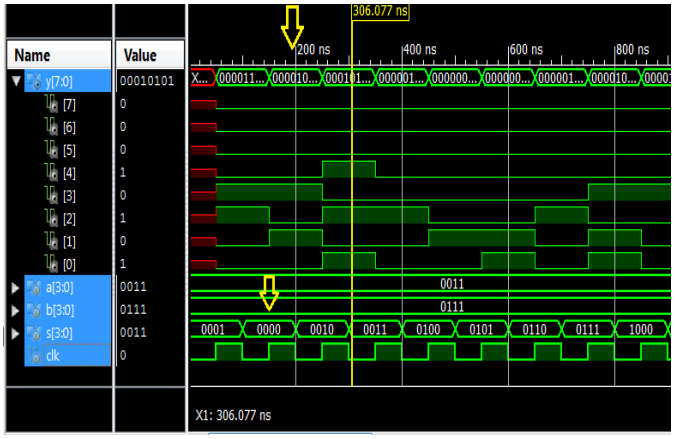


Fig 14: Addition of two binary numbers

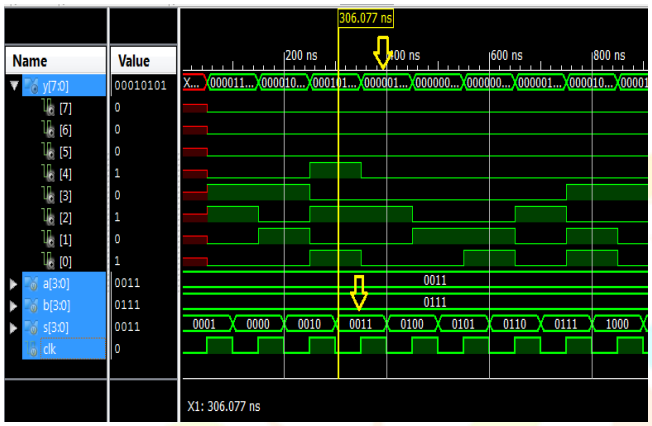


Fig 15: Increment of two binary numbers

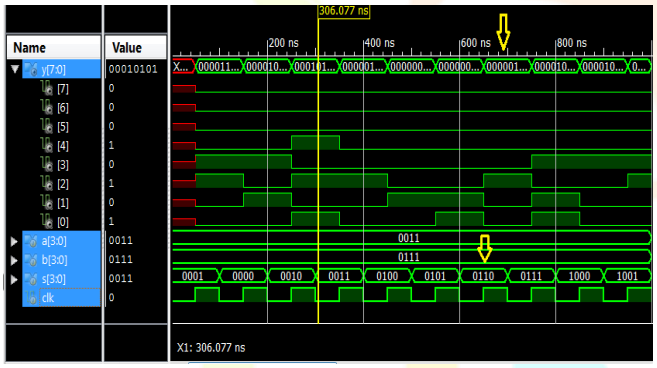
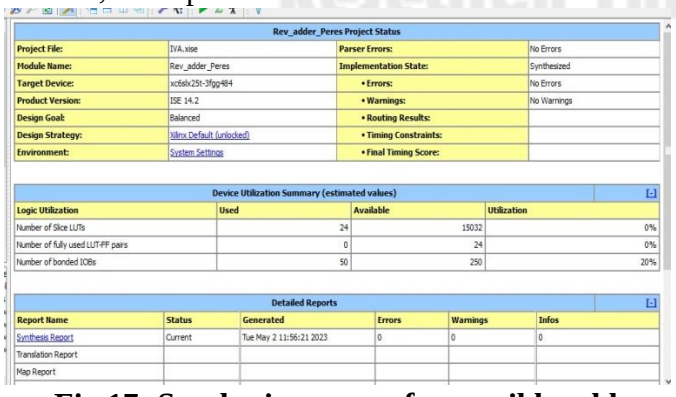


Fig 16: XOR of two binary numbers

3.4 SYNTHESIS RESULTS

Below figures Fig 17, Fig 18, Fig 19 represents the Synthesis results of the proposed circuits, Adder, Multiplier and ALU.



Rev_adder_Peres Project Status

Project File:	IVA.xise	Parser Errors:	No Errors
Module Name:	Rev_adder_Peres	Implementation State:	Synthesized
Target Device:	xc6slx25t-3fgg484	• Errors:	No Errors
Product Version:	ISE 14.2	• Warnings:	No Warnings
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

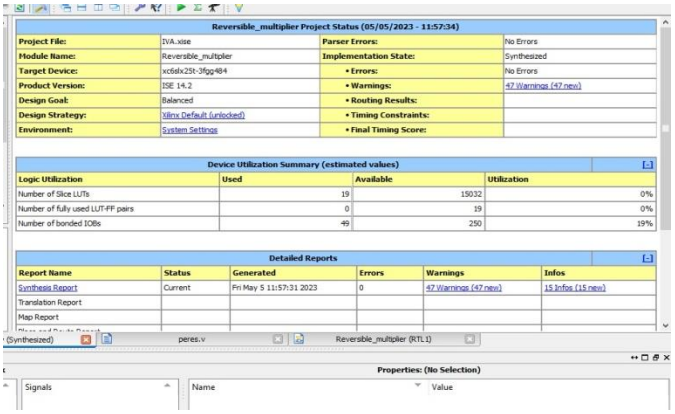
Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	24	15032	0%
Number of fully used LUT-FF pairs	0	24	0%
Number of bonded IOBs	50	250	20%

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Tue May 2 11:56:21 2023	0	0	0
Translation Report					
Map Report					

Fig 17: Synthesis report of reversible adder



Reversible_multiplier Project Status (05/05/2023 - 11:57:34)

Project File:	IVA.xise	Parser Errors:	No Errors
Module Name:	Reversible_multiplier	Implementation State:	Synthesized
Target Device:	xc6slx25t-3fgg484	• Errors:	No Errors
Product Version:	ISE 14.2	• Warnings:	47 Warnings (47 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

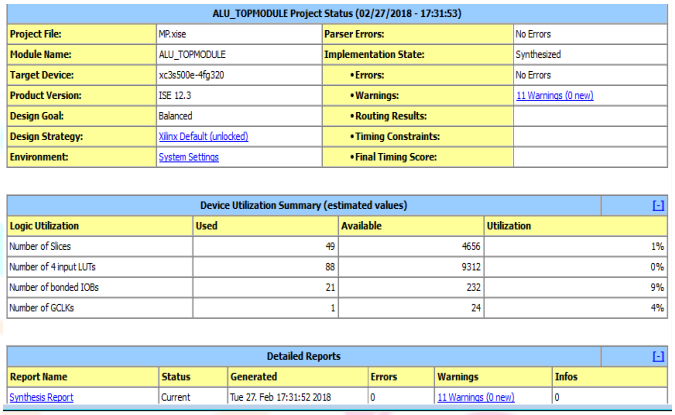
Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	19	15032	0%
Number of fully used LUT-FF pairs	0	19	0%
Number of bonded IOBs	49	250	19%

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Fri May 5 11:57:31 2023	0	47 Warnings (47 new)	15 Infos (15 new)
Translation Report					
Map Report					

Fig 18: Synthesis report of reversible multiplier



ALU_TOPMODULE Project Status (02/27/2018 - 17:31:53)

Project File:	MP.xise	Parser Errors:	No Errors
Module Name:	ALU_TOPMODULE	Implementation State:	Synthesized
Target Device:	xc3s500e-4fg320	• Errors:	No Errors
Product Version:	ISE 12.3	• Warnings:	11 Warnings (0 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	49	4656	1%
Number of 4 input LUTs	88	9312	0%
Number of bonded IOBs	21	232	9%
Number of GCLKs	1	24	4%

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Tue 27. Feb 17:31:52 2018	0	11 Warnings (0 new)	0

Fig 19: Synthesis report of reversible ALU

4.COMPARISION

Table showing the comparison of various circuits designed by using basic logic gates and using reversible gates.

Circuit	Delay using logic gates (ns)	Delay using reversible gates (ns)
16-bit Adder	14.236	12.210
16x16 Multiplier	9.557	7.832
ALU	16.368	14.642

5. CONCLUSION

The proposed Adder, Multiplier and ALU design has been designed and modeled using Verilog HDL and verified using Xilinx tool. ALU design has a four-bit control signal to perform six arithmetic and ten logical operations. The proposed ALU design uses both reversible and semi reversible gates in it. Arithmetic operations are addition, subtraction, multiplication, increment and decrement. Logical operations are AND gate, OR gate, NOT gate, NAND gate, NOR gate, XOR gate, XNOR gate, a'b. The operations are performed based on four control bits using multiplexer. Total of sixteen operations are performed by the proposed ALU. The Reversible Adder, Multiplier and ALU designs occupy less area and consume less power compared to conventional logic gates design approach. The proposed

designs are coded in Verilog HDL followed by synthesization and simulation using Xilinx ISE 14v tool.

6. REFERENCES

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