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Design of PLL Using Low Power Applications

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***Abstract*-The project proposes the design of a phase-locked loop (PLL) using an improved performance ring voltage-controlled oscillator (VCO). The modified ring VCO topology incorporates a tail current source and cross-coupled transistors to enhance linearity and reduce phase noise. The design is implemented using a 45nm CMOS process and simulations are conducted using Tanner EDA. The proposed design shows improved performance compared to conventional PLLs, making it well-suited for high-performance communication systems. The results validate the effectiveness of the modified ring VCO topology in enhancing the performance of PLL-based applications.**

KEYWORDS - VCO, Phase Locked Loop,Tanner EDA,Phase Noise

INTRODUCTION

A Phase Locked Loop is a closed loop feedback control system which is capable of generating a clock signal that has a fixed relationship to the reference clock signal. It causes a particular system to track with another one. The PLL technique is active around for a long time. It has various applications include keeping power generators in phase, synchronizing to the pulse in a TV set, clock recovery from asynchronous data, demodulating an FM modulated signal and so on. Although there are legitimate applications, the primary use is frequency synthesis. The General block diagram of the PLL is illustrated in Figure 1. The primary function of the PLL is the VCO's output using externally present reference signal and output of the frequency divider. Both signals are in phase with each other. Further, the VCO's output indicates that the phase difference between both the signals is constant with respect to time.

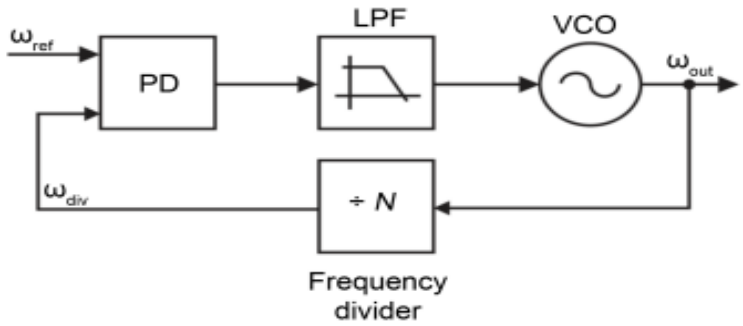

Fig 1 Block diagram of the PLL

An essential module in the PLL is the Phase Detector (PD) or PFD. It compares the reference frequency signal with the

signal fed back from output of the VCO, and the difference signal is used as an input to both the loop filter and the VCO. In digital PLL (DPLL), the logical element is the PFD and the competence of the PFD produces a zero dead zone that leads to an attractive recording and locking performance in the PLL.

Literature Review

In this section, a brief introduction of the work that has been done with respect to this field is discussed.

In this paper [1],Phase-locked loops (PLLs) have been widely used in high-performance microprocessors and high-speed digital communication systems as clock generators. As the speed of these systems is increasing, PLLs with higher operating frequency and lower jitter are in demand. A common architecture for clock generation uses a phase-frequency detector (PFD) for simultaneous phase and frequency acquisition. Generating a high-frequency clock increases the difficulty of the design of the PFDs, particularly for systems with a high input clock frequency and minimum frequency multiplication.

The Author in paper [2], The adoption of dynamic dividers in CMOS phase-locked loops for multi-gigahertz applications allows to reduce the power consumption substantially without impairing the phase noise and the power supply sensitivity of the phase-locked loop (PLL). A 5-GHz frequency synthesizer integrated in a 0.25-/spl mu/m CMOS technology demonstrates a total power consumption of 13.5 mW. The frequency divider combines the conventional and the extended true-single-phase-clock logics. The oscillator employs a rail-to-rail topology in order to ensure a proper divider function. This PLL intended for wireless LAN applications can synthesize frequencies between 5.14 and 5.70 GHz in steps of 20 MHz. The reference spurs at 10-MHz offset are as low as -70 dBc and the phase noise is lower than -116 dBc/Hz at 1 MHz over the whole tuning range.

In this paper [3], it describes an I/O scheme for use in a high-speed bus which eliminates setup and hold time requirements between clock and data by using an oversampling method. The I/O circuit uses a low jitter phase-locked loop (PLL) which suppresses the effect of supply noise. Measured results show peak-to-peak jitter of 150 ps and R.M.S. jitter of 15.7 ps on the clock line. Two experimental chips with 4-pin interface have been fabricated with a 0.6 /spl mu/m CMOS technology, which exhibits the bandwidth of 960 Mb/s per pin.

The Author in paper [4], describes the Tri-state digital phase-frequency detectors (PFDs) are widely used for the large capture and locking range that they enable, but suffer from relatively large in-band phase noise. Sub-sampling phase detectors have recently been demonstrated to offer very low in-band noise but with only a very small capture range. We show how a PFD and a sub-sampling phase detector can be combined to maintain the phase-frequency detection capabilities while simultaneously obtaining in-band noise suppression. A 2.2GHz PLL is demonstrated in a 65nm CMOS process with an on-chip loop filter area of 0.04mm2. The measured in-band phase noise improves from −110dBc/Hz to −122dBc/Hz when the auxiliary sub-sampling phase detector is active.

In this paper [5], As the key blocks of PLL (phase locked loop) circuits, PFD (Phase Frequency Detector) is dominated to the precision and stability of system, whereas CP (Charge Pump) offers a wide scale of frequency capture scale and fast locked performance. The structure of PFD using transfer gate dynamic D flip-flops and the structure with a wide input scale

error amplifier for CP had been presented to achieve a high performance.

In the end, the chip was taped out in the process of TSMC 0.18μm CMOS. The post-simulation results show that the PFD has correct logic function, whereas the charge pump current is stable at 100μA in the output range of 0.2V~0.8V, and the current mismatch is less than 0.4μA at output voltage range of 0.2V~0.8V, with total power consumption of 3mW with the power supply of 1V.

In this paper [6], A high-speed CMOS phase/frequency detector (PFD) for faster frequency acquisition is presented. An improved CMOS D-type master-slave flip-flop is described and adopted. Higher speed is attributed to the reduced node capacitances. Charge-sharing phenomena are circumvented. An input delay scheme is employed to achieve faster acquisition. The optimal delay for PFD maximum operating frequency is analytically studied and a design guide is given.

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In this paper [8], the author introduces a modified design of Phase frequency detector (PFD) with reduced dead zone and improved charge pump (CP) with reduced current mismatch for a Phase Locked Loop (PLL). Three modified PFD circuits are proposed, designed, simulated, and the results are analyzed considering dead zone as a constraint. Design of pass transistor logic network plays a part in the diminution of the dead zone. Further, an improved design of CP is proposed to reduce current mismatch. It is achieved by placing the single ended differential amplifier in current– voltage feedback configuration which offers high output impedance. Simulations are performed using T-SPICE, implemented in IBM 0.13 μm technology under 1.3 V power supply. Results show that the modified PFD design has a dead zone of 0.3 ns and the current mismatch decrements to 0.1 μA in an improved CP design.

In this paper [9], the author presents the design and implementation of a Phase Locked Loop (PLL) using a low power ring Voltage Controlled Oscillator (VCO) with improved performance. The proposed PLL is suitable for use in GHz frequency range communication systems and has several attractive features such as structural simplicity, good dynamic response, low power consumption, small area, and a great potential for use in implantable biomedical and wireless systems. The PLL's components are designed using a multiplexer for the Phase Frequency Detector (PFD), switched capacitor technique for the Low Pass Filter (LPF), and a current starved voltage controlled ring oscillator for the VCO. Simulation results demonstrate the effectiveness of the proposed design.

Phase locked loop operation

The basic concept of the operation of the PLL is relatively simple, although the mathematical analysis and many elements of its operation are quite complicated

The diagram for a basic phase locked loop shows the three main element of the PLL: phase detector, voltage controlled oscillator and the loop filter.

In the basic PLL, reference signal and the signal from the voltage controlled oscillator are connected to the two input ports of the phase detector. The output from the phase detector is passed to the loop filter and then filtered signal is applied to the voltage controlled oscillator.

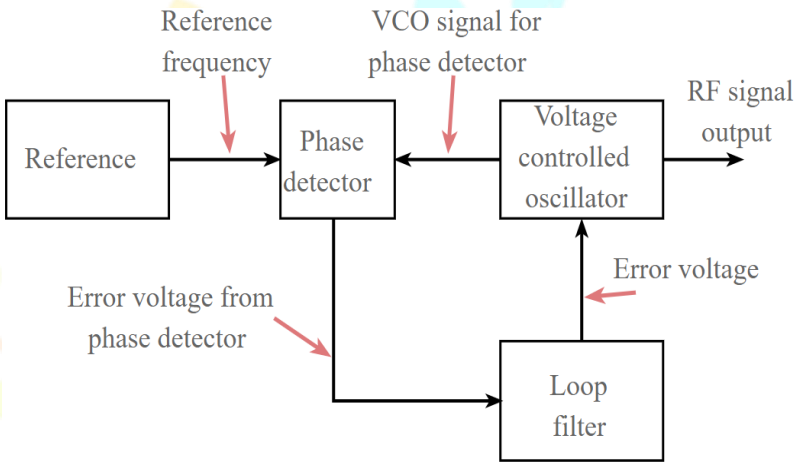

Fig 2 Phase loop Lock Diagram showing voltages

The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals.

The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal. Once through the filter the error signal is applied to the control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked.

When the PLL, phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency.

The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency.

Methadology

In this project it reports a new proposal of a modified circuit for PFD in order to reduce the dead zone and combined with other modules to obtain PLL output.It is observed that the internal signal routing is required to reduce the dead zone in the PFD circuit. Based on that concept, the high-speed dynamic PFD is proposed (PPFD) and designed.The reset path of PFD is eliminated by routing the PFD input connections to the flip-flop that is located next to it. The input of one flip-flop plays a role in developing reset signal for the other flip flop.Thereby the dead zone is eliminated and the power is decreased by reducing a transistor from the existing circuit of the High speed dynamic PFD.Reducing the number of transistors, the area is decreased, and the speed of the circuit is increased. It overcomes the inaccuracy of the PFD output when the reference signal leads the VCO signal as the design is minimized.With the aid of smallest channel length in the circuit design, it confesses as an explicit device that is shrinking with the scaling of CMOS technology.This operation is said to be a Phase lock-in. After addition, the PLL achieves the phase-locked condition, where PLL tracks the input.Under this condition, VCO frequency is equal to the input frequency. The overall PLL design is presented with every external input pulse so that the feedback VCO and the external input clock are matched, the circuit then locks onto itself within a narrow frequency band.If the clock of entry varies slightly, the PLL frequency does not change. This narrow frequency band is the dead zone of the PPFD. Within this zone, the VCO signal and reference signal are so close in-phase that there are no correction pulses out of the PPFD circuit. Once the phase shifts out of this frequency band, the PPFD is correcting again. As the PLL design is functioning properly, it is extended further by connecting with Frequency divider (FD) blocks. This Project is being implemented on Tanner EDA tool using 45nm technology.

Conclusion

In this paper it introduces a modified PLL design with an improved ring VCO and PPFD circuit. The modifications enhance performance, reduce the dead zone, and improve accuracy. The proposed design achieves wide frequency range, frequency tunability, and low power consumption. Simulations validate the superior performance of the design. Overall, the paper presents an effective solution for precise frequency control and synchronization in communication systems.

References

[1].M. Mansuri, D. Liu and C. . -K. K. Yang, "Fast frequency acquisition phase- frequency detectors for Gsamples/s phase-locked loops," in IEEE Journal of Solid- State Circuits, vol. 37, no. 10, pp. 1331-1334, Oct. 2002, doi: 10.1109/JSSC.2002.803048.

[2].S. Pellerano, S. Levantino, C. Samori and A. L. Lacaita, "A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic frequency divider," in IEEE Journal of Solid-State Circuits, vol. 39, no. 2, pp. 378-383, Feb. 2004, doi: 10.1109/JSSC.2003.821784.

[3].Sungjoon Kim, Kyeongho Lee, Yongsam Moon, Deog-Kyoon Jeong, Yunho Choi and Hyung Kyu Lim, "A 960-Mb/s/pin interface for skew-tolerant bus using low jitter PLL," in IEEE Journal of Solid-State Circuits, vol. 32, no. 5, pp. 691-700, May 1997, doi: 10.1109/4.568836.

[4].C. -w. Hsu, K. Tripurari, S. -A. Yu and P. R. Kinget, "A 2.2GHz PLL using a phase-frequency detector with an auxiliary sub-sampling phase detector for in-band noise suppression," 2011 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 2011, pp. 1-4, doi: 10.1109/CICC.2011.6055307.

[5].F. Xiangning, L. Bin, Y. Likai and W. Yujie, "CMOS Phase Frequency Detector and Charge Pump for Wireless Sensor Networks," 2012 IEEE MTT-S International Microwave Workshop Series on Millimeter Wave Wireless Technology and Applications, Nanjing, China, 2012, pp. 1-4, doi: 10.1109/IMWS2.2012.6338217.

[6].R. Y. Chen and H. -Y. Huang, "A High-speed Fast-acquisition CMOS Phase/Frequency Detector for MB-OFDM UWB," 2007 Digest of Technical Papers International Conference on Consumer Electronics, Las Vegas, NV, USA, 2007, pp. 1-2, doi: 10.1109/ICCE.2007.341324.

[7].Soh, L.K., Sulaiman, M.S. and Yusof, Z. (2008) A Fast Lock Delay-Locked Loop Architecture with Improved Precharged PFD. Journal of Analog Integrated Circuits Signal Process

[8].ANUSHKANNAN, N.K., MANGALAM, H. Design of a CMOS PFD-CP module for a PLL. Sadhana 40, 1105–1116 (2015).
https://doi.org/10.1007/s12046-015-0379-1

[9].S. Suman, K. G. Sharma and P. K. Ghosh, "Design of PLL using improved performance ring VCO," 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, India, 2016, pp. 3478-3483, doi: 10.1109/ICEEOT.2016.7755351.