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Multilevel Inverter Topology with Level-Shifted PWM Technique for PV Application.

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Abstract: As per the literature study of existing inverter topologies, multilevel inverters continue to be an area of research interest. It remains difficult to maintain a sinusoidal stepped output while lowering the switch count and stress on the power electronics switches. A 15-level multilevel inverter for photovoltaic application is shown in the study. The multilevel inverter's asymmetrical flying capacitor topology is studied in the system. The inverter uses a level-shifted PWM modulation approach. With the aid of simulation in the MATLAB/SIMULINK environment, the major goal of the research is to investigate and analyze modulation technique, voltage stress across switches, and Total Harmonic Distortion (THD) of output voltage.

IndexTerms - Inverter, level-shifted PWM, PV, THD

I.INTRODUCTION

The global energy scenario is constantly evolving and facing numerous challenges. With the increasing global demand for energy, concerns over energy security, climate change, and environmental degradation are becoming more pressing. Renewable energy sources such as solar, wind, hydro, and geothermal are gaining momentum as viable alternatives to traditional fossil fuels. However, the transition to clean energy is complex, and there are still many hurdles to overcome, including the high initial costs of renewable energy infrastructure, energy storage, and the need for policy frameworks that support the deployment of renewable energy technologies. Despite these challenges, there is growing momentum towards a sustainable energy future, driven by a combination of technological advancements, policy incentives, and changing consumer preferences [1].

Solar panels are used in the PV (photovoltaic) power generation process, which turns sunlight into electricity. Direct current (DC) power is produced by photovoltaic cells found in solar panels by absorbing sunlight. An inverter is a device employed to convert direct current (DC) electricity into alternating current (AC) electricity, enabling its utilization for residential, commercial, and even large-scale power supply purposes. Because most electrical appliances use AC power instead of DC power produced by solar panels, inverters are required. In addition to converting DC to AC power, inverters also manage the voltage and frequency of the electricity to ensure that it is compatiblewith the grid and devices being powered. Modern inverters also have advanced features such as monitoring systems that allow users to track energy production and consumption, and smart grid integration that enables PV systems to communicatewith the electrical grid. The effectiveness and dependability ofthe inverter are crucial to a PV system's overall performance, and advances in inverter technology are contributing to the widespread adoption of solar energy around the world [2][3]. Multilevel inverters being used in PV (photovoltaic) power generation systems due to their ability to produce high-qualityAC (alternating current) voltage output that is well suitedfor grid-connected PV systems. This is important because harmonic distortion can cause damage to electrical equipment,and it can also interfere with other electrical devices on the grid. Multilevel inverters can also improve the efficiency of PV systems by enabling the use of higher voltage and lower current, which can reduce losses in the system and improvethe overall energy yield [4][5].

While multilevel inverters offer numerous advantages for PV (photovoltaic) power generation systems, they are not without limitations. One of the main limitations of multilevel inverters is their high cost compared to conventional inverters.This is because multilevel inverters require a larger numberof components, such as capacitors and switches, this can lead to an elevation in the overall system expenses. Additionally, multilevelinverters can be more complex to design and control, which can increase the risk of failures and require more specialized knowledge to install and maintain. Another limitationof multilevel inverters is their lower efficiency compared to conventional inverters at low power levels. This is becausethe additional components in multilevel inverters can introduceadditional losses, which can reduce the overall efficiency of the system. Despite these limitations, multilevel inverters are still an important technology for improving the performance and reliability of PV systems, and ongoing research and development is focused on addressing these limitations and improving the overall performance of multilevel inverters for PV applications [6].

II. Topologies for Multilevel Inverter

A 15-level multilevel inverter is an electronic device used to convert a direct current (DC) voltage into an alternating current (AC) voltage with the ability to produce 15 distinct voltage levels. It achieves this by using a series of capacitors and switches to create a staircase-like waveform with multiple voltage steps. The 15-level multilevel inverter can produce a high-quality AC waveform that is nearly sinusoidal, which is important for reducing harmonic distortion and improving the overall power quality of the system

[7]. There are several different topologies of 15-level multilevel inverters, each with their own advantages and disadvantages. Some of the most common topologies include:

1. Cascaded H-Bridge Inverter (CHB)

This topology is extensively employed in multilevel inverters and is characterized by multiple H-bridge inverters interconnected in series, each generating a distinct voltage level. The configuration, illustrated in Fig. 1, offers modularity and simplicity in control. However, it necessitates a significant number of components, potentially resulting in higher costs. [8].

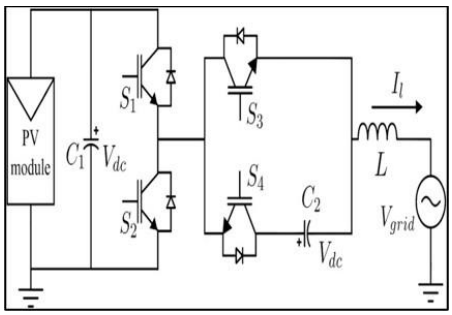

Fig. 1. Cascaded H-Bridge Topology

2. Neutral Point Clamped Inverter (NPC)

This topology uses a clamping circuit to maintain the voltage at the neutral point of the DC source. As per shown in Fig. 2, it is a simple and efficient topology, but it requires a large number of switches and can be difficult to control [9].

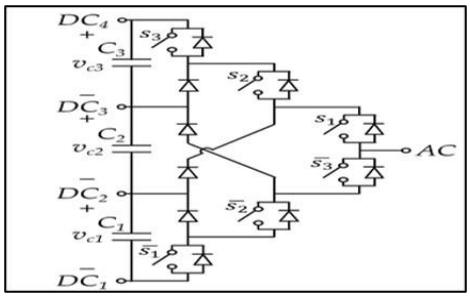

Fig. 2. Neutral Point Clamped Topology

3. Flying Capacitor Inverter (FC)

This topology uses capacitors that "fly" between voltage levels to produce the AC waveform. It is a relatively simple and cost-effective topology, but it can be difficult to control and requires a large number of capacitors as per described in Fig. 3 [10].

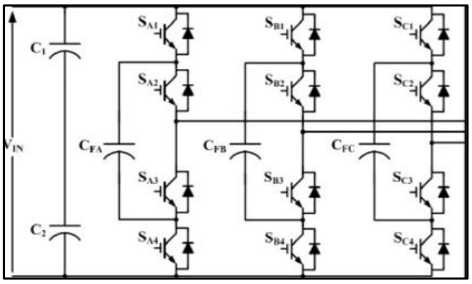

Fig. 3. Flying capacitor topology

Overall, each topology has its own strengths and weak-nesses, and the choice of topology will depend on the specific requirements of the application.

III. Modulation Techniques for Multilevel Inverter

Modulation techniques are used to control the switches in a multilevel inverter and generate the desired AC waveform. Some of the common modulation techniques for multilevel inverters include [12].

1. Carrier-Based Pulse Width Modulation (PWM): For multilevel inverters, this is the modulation method that is most frequently utilised. It entails creating a PWM signal from the difference between two signals by comparing a high-frequency carrier waveform with a reference signal. To produce the desired AC waveform, the inverter's switches are controlled by the PWM signal.
2. Level-Shifted Pulse Width Modulation (PWM): This technique uses two carriers with a phase shift to generate a PWM signal that controls the switches in the inverter. This method lowers switching losses and boosts the inverter's effectiveness.
3. Space Vector Pulse Width Modulation (PWM): This technique uses a three-phase reference signal and a carrier signal to generate a space vector that controls the switches in the inverter. This technique is efficient and can produce a high-quality AC waveform with low harmonic distortion.

4. Selective Harmonic Elimination (SHE): This method uses the inverter's switching angles to remove particular harmonics from the output waveform. This technique can produce a high-quality AC waveform with very low harmonic distortion, but it can be complex and time-consuming to implement [13].

Advantages of Modulation Techniques

Modulation techniques play a critical role in controlling the switches in a multilevel inverter and generating the desired AC waveform. Some of the advantages of using modulation techniques in multilevel inverters include:

1. High-quality output waveform: Modulation techniques al- low for precise control of the inverter switches, which can produce a high-quality AC waveform with low harmonic distortion and improved power quality.
2. Efficient operation: By controlling the switches in the inverter, modulation techniques can reduce switching losses, improve efficiency, and minimize heat dissipation.
3. Flexibility: Different modulation techniques can be used to produce a wide range of output waveforms and accommodate various load types and operating conditions.
4. Easy implementation: Many modulation techniques are straightforward to implement and can be easily integrated into existing multilevel inverter systems.

Limitations of Modulation Techniques

While modulation techniques offer many advantages for controlling multilevel inverters, there are also some potential disadvantages that should be considered. Some of the dis- advantages of modulation techniques in multilevel inverters include:

1. Complexity: Some modulation techniques can be com- plex to implement, requiring sophisticated algorithms, hardware, or software. This complexity can increase the cost and time required to design and build the inverter system.
2. Computational requirements: Many modulation techniques require real-time computation of complex algorithms, which can be challenging for some systems. This can increase the hardware and software requirements of the inverter system and may impact its performance.
3. Switching losses: While modulation techniques can reduce switching losses in multilevel inverters, they may also introduce additional switching losses due to the complex switching patterns and control algorithms.
4. Harmonic distortion: Some modulation techniques may introduce harmonic distortion in the output waveform due to the non-linear switching patterns and control algorithms.

IV. Level Shifted PWM Technique.

Level-Shifted Pulse Width Modulation (PWM) is a modulation technique used in multilevel inverters to control the switching of power semiconductor devices. This technique can produce high-quality output waveforms with low harmonic distortion and reduced switching losses. In this article, we will provide a detailed overview of Level-Shifted PWM, its working principle, advantages, and applications [14].

Working Principle of Level-Shifted PWM

Level-Shifted PWM is a variation of Carrier-Based PWM, which is a popular modulation technique used in multilevel inverters. In Carrier-Based PWM, a high-frequency carrier signal is compared to a reference signal to generate the switching signals for the inverter switches. However, in Level- Shifted PWM, the reference signal is shifted by a certain level, known as the DC offset voltage, before being compared to the carrier signal. The DC offset voltage is typically set to half of the voltage level of the highest level in the multilevel inverter. This ensures that the switching signals for the highest-level switches are always active, which helps to reduce the voltage stress on the other switches. The carrier signal is typically a triangular wave with a fixed frequency, which is generated by a separate oscillator circuit. The output waveform of a Level- Shifted PWM inverter consists of a series of stepped voltage levels, which are proportional to the amplitude of the reference signal.

V. Analysis

In, the Fig. 4, 15 level multilevel inverter simulated circuit diagram is shown. The inverter is made up of two FCs (C1 and C2) and 11 switches (S1-S11) are connected to load. The DC link voltage are defined as Vdc. There are three separate voltage sources with the names Vdc1, Vdc2, and Vdc3. There are three diodes in the inverter: D1, D2, and D3. Ten power MOSFETs, S1-S2, S4-S11, and one power IGBT, S3 is present with absence of anti-parallel diode [15].

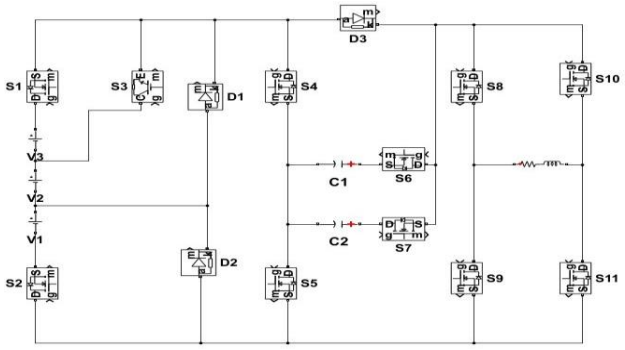

Fig. 4. Circuit schematic of 15-level inverter studied in paper

Switching operation-

1. Positive Half cycle: Table 1, denotes the truth table for switching patterns for positive half cycle of the 15-level multilevel inverter. All the levels for positive half cycles are discussed below. Here the VR = Voltage across load.

Table no. I: Switching sequence for positive half cycle

	0	1	2	3	4	5	6	7

S1	0	0	0	0	1	1	1	1
S2	0	1	0	1	0	1	1	1
S3	0	0	1	1	0	0	0	0
S4	0	0	0	0	0	0	1	1
S5	0	1	1	0	0	0	0	0
S6	0	1	0	0	0	0	1	0
S7	0	0	1	0	0	0	0	1
S8	1	1	1	1	1	1	1	1
S9	0	0	0	0	0	0	0	0
S10	1	0	0	0	0	0	0	0
S11	0	1	1	1	1	1	1	1

Level 0: A short circuit occurs when the switches S8 and S10 are ON, or S9 and S11 are ON but all the other switches are OFF. VR = 0in this scenario.
Level 1: In the provided level, switches S2, S5, S6, S8, and S11 are all on, while diode D2 and D3 are both facing forward and the rest of the switches are all off. The capacitor C1 is charged at this level. VR = 100V in this scenario.
Level 2: In the specified level, switches S3, S5, S7, S8, and S11 are turned on, while diodes D1 and D3 are pointed forward and all other switches are off. The capacitor C2 is charged at this level. VR = 200V in this scenario.
Level 3: In the provided level, switches S2, S3, S8, and S11 are all turned on, but only diode D3 is moving forward while all other switches are off. VR = 300V in this scenario.
Level 4: In the provided level, switches S1, S8, and S11 are turned on, while diodes D1 and D3 are pointed forward and all other switches are off. VR = 400V in this scenario.
Level 5: In the provided level, switches S1, S2, S8, and S11 are all turned on, while diode D3 is pointing forward and all other switches are off. In this scenario, VR = 500V.
Level 6: All other switches are off in the level, except for S1, S2, S4, S6, S8, and S11. The capacitor C1 is discharged at this point, assisting in the level boost. VR = 600V in this scenario.
Level 7: All other switches are off throughout the level, save for switches S1, S2, S4, S7, S8, and S11. The capacitor C2 discharges at this point and aids in boosting a higher level. VR = 700V in this circumstance.

2. Negative Half cycle: Table 2, denotes the truth table for switching patterns for negative half cycle of the 15-level multilevel inverter. All the levels for negative half cycles are discussed below.
Level 1: In the provided level, switches S2, S5, S6, S10, and S9 are on, while diode D2 and D3 are both facing forward and the rest of the switches are all off. The capacitor C1 is charged at this level. VR = -100V in this scenario.
Level 2: In the specified level, switches S3, S5, S7, S10, and S9 are turned on, while diodes D1 and D3 are pointed forward and all other switches are off. The capacitor C2 is charged at this level. VR = -200V in this scenario.
Level 3: In the provided level, switches S2, S3, S10, andS9 are all turned on, but only diode D3 is moving forward while all other switches are off. VR = -300V in this scenario.
Level 4: In the provided level, switches S1, S10, and S9are turned on, while diodes D1 and D3 are pointed forward and all other switches are off. VR = -400V in this scenario.

Table no. II: Switching sequence for negative half cycle

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
S1	*0*	0	0	0	1	1	1	1
S2	0	1	0	1	0	1	1	1
S3	0	0	1	1	0	0	0	0
S4	0	0	0	0	0	0	1	1
S5	0	1	1	0	0	0	0	0
S6	0	1	0	0	0	0	1	0
S7	0	0	1	0	0	0	0	1
S8	1	0	0	0	0	0	0	0
S9	0	1	1	1	1	1	1	1
S10	1	1	1	1	1	1	1	1
S11	0	0	0	0	0	0	0	0

Level 5: In the provided level, switches S1, S2, S10, andS9 are all turned on, while diode D3 is pointing forward andall other switches are off. In this scenario, VR = -500V.
Level 6: All other switches are off in the level, except for S1, S2, S4, S6, S10, and S9. The capacitor C1 is discharged at this point, assisting in the level boost. VR = -600V in this scenario.
Level 7: All other switches are off throughout the level, save for switches S1, S2, S4, S7, S10, and S9. The capacitor C2 discharges at this point and aids in boosting a higher level. VR = -700V in this circumstance.

The dc-link voltage is increased to 700V for the inverter with three input dc voltages of 100V, 200V, and 200V. The switching frequency across all switches is 10 kHz. The output voltage and current are also relatively constant and stable. In Fig. are additional waveforms demonstrating voltage stress across the switches. The maximum voltage across the switches is 700V, which is the same

as the dc-link voltage. The resistor's value is 280 Ohm for solely resistive loads and 200 Ohm with a 200 mH inductor for resistive-inductive loads [16].

V. Results from simulation

The reduction of overall harmonic distortion has not been discussed since the goal of this work is to study a multilayer inverter with modulation technique. The study provides results for 15-level multilevel inverters, where simulations were conducted to model the inverter and synthesize a specific load voltage waveform.

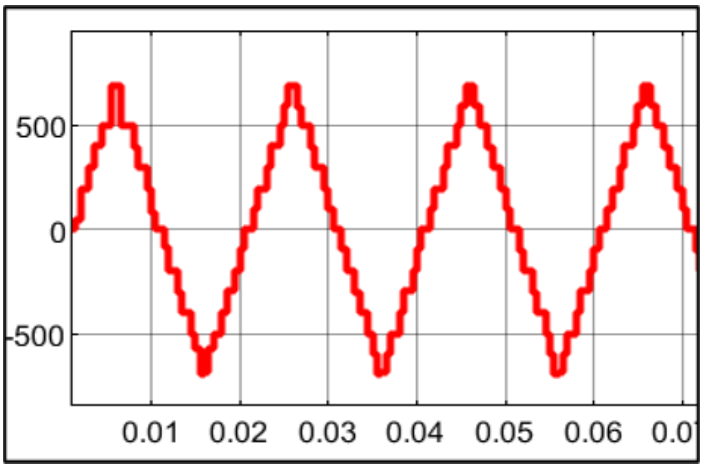

Fig. 5. Stepped Output Voltage Waveform

Due to the values 100V, 200V and 200V of the DC voltage sources employed in this study, a 15-level inverter can produce staircase voltage waveforms with maximum values of 700V as shown in Fig 5.

In the simulation, two distinct loads are connected to the multilevel inverters. Figure 7 illustrates the current behavior of a 15-level multilevel inverter when solely resistive load is applied. The current waveform exhibits a stepped pattern and maintains a power factor of unity.

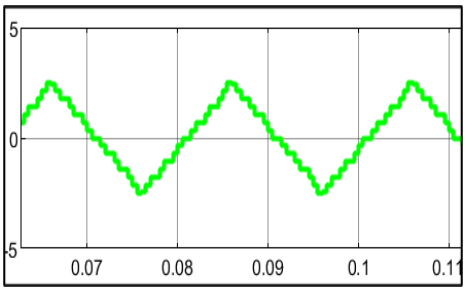

Fig. 6. Current with resistive load

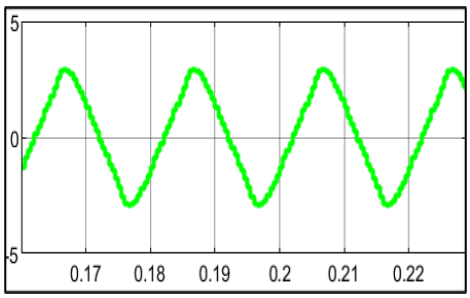

Fig. 7. Current with resistive-inductive load

In Fig. 7, the current behavior of a 15-level multilevel inverter is depicted for an R-L load. While the output voltage remains unchanged as shown in Figure 5, the presence of the inductive load causes the output current to exhibit a sinusoidal waveform with a fundamental frequency. Fig. 8 and 9, shows that the voltage waveforms across the capacitors C1 and C2 respectively.

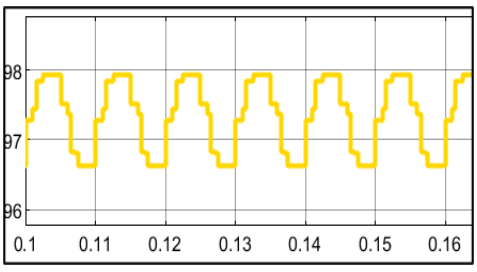

Fig. 8. Voltage across Capacitor (C1)

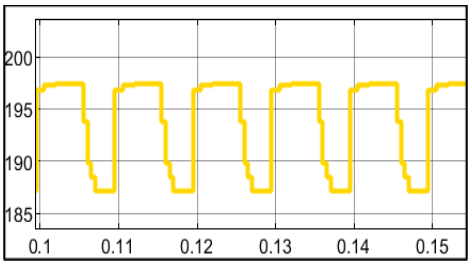

Fig. 9. Voltage across Capacitor (C2)

Fig. 10 and 11, shows that the voltage waveforms acrossthe diodes D1 and D3 respectively.

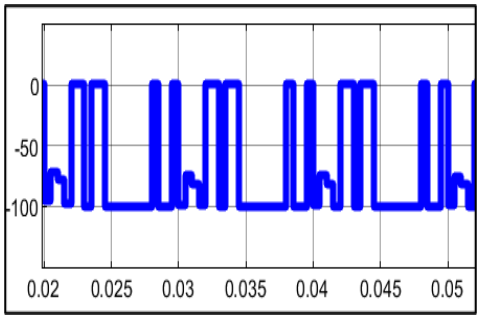

Fig. 10. Voltage across Diode (D1)

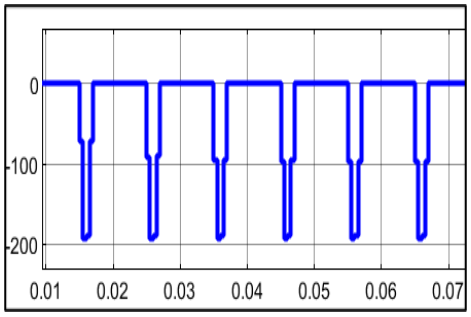

Fig. 11. Voltage across Diode (D3)

Fig.12 and 13, shows that the voltage waveform i.e., voltage stress across the switches S1 and S2 respectively.

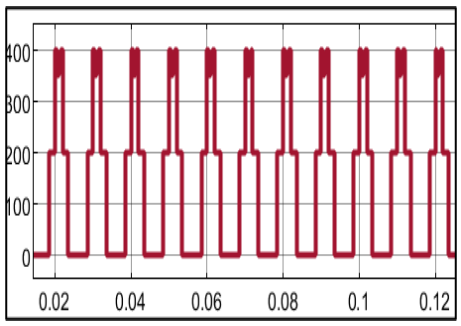

Fig. 12. Voltage stress across S1

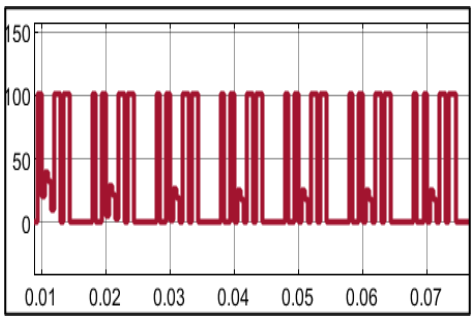

Fig. 13. Voltage stress across S2

Fig.14 and 15, shows that the voltage waveforms across the switches S3 and S5 respectively.

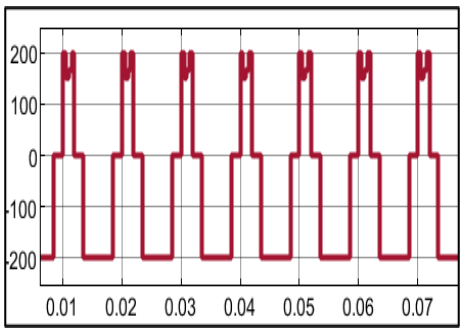

Fig. 14. Voltage stress across S

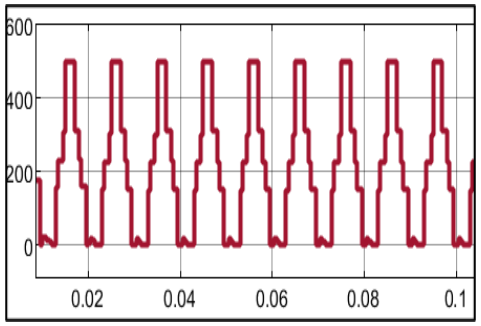

Fig. 15. Voltage stress across S3

Fig. 16 and 17, shows that the voltage waveforms across the switches S8 and S10 respectively.

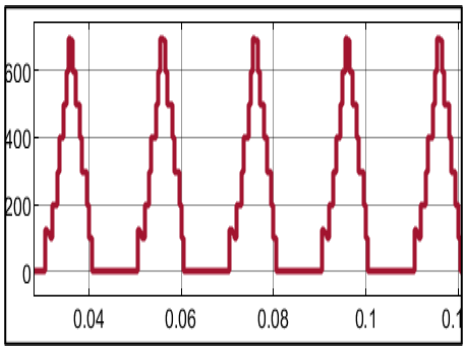

Fig. 16. Voltage stress across S8

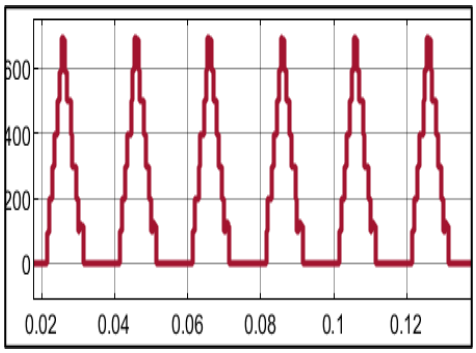

Fig. 17. Voltage stress across S10

Fig. 18, shows THD analysis of a 15-level multilevel inverter performed by simulating the circuit using software MATLAB/Simulink. It is necessary to analyze the THD of a 15-level multilevel inverter to guarantee the quality of the output waveform and the execution of the system. As per shown in Fig. the THD value for output voltage is 14.89 percent for given R-L loading condition.

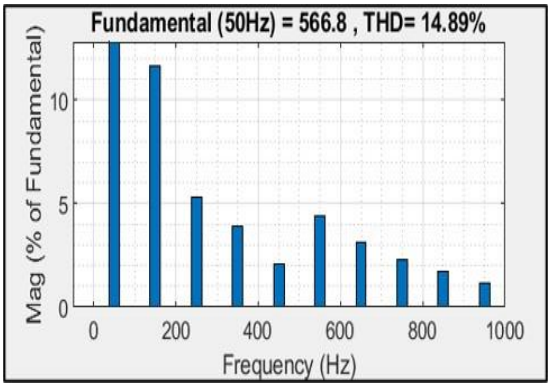

Fig. 18 THD analysis for output voltage

VI. Conclusion-

A 15-level multilevel inverter is that it can produce a high- quality output voltage that closely approximates a sine wave, which is important for many applications, including motor drives and renewable energy systems. Some topologies of multilevel inverter and the prominent modulation techniques techniques discussed. Working-principle, advantages and ap- plications of level-shift PWM technique is also discussed. In this paper, 15-level Multilevel inverter is simulated with level- shift PWM modulation technique. The operating principle is discussed for all the switching states. This is followed with some basic simulation results which includes 15 level output voltage waveform, and voltage stress waveform across the switches, diodes and capacitors. Also the Total Harmonic Distortion is calculated through FFT analysis.

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