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FPGA Design of Effective Detection Low Power Architecture for Recycled ICs

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Abstract : The counterfeiting and exercise of integrated circuits (ICs) became major problems in recent years, doubtless impacting the safety and dependableness of electronic systems sure for military, financial, or alternative crucial applications. With identical practicality and packaging, it\'d be very troublesome to differentiate recycled ICs from unused ICs. In this paper, two varieties of on-chip light-weight sensors area unit planned to identify recycled ICs by measurement circuit usage time once utilized in the sector. Recycled ICs detection supported aging in Ring Oscillators (ROs-based) and Anti-Fuse (AF-based) square measure the two techniques given during this paper. The planned methodology is meant mistreatment Verilog compound, simulated mistreatment Modalism and synthesized pattern Xilinx code.

***IndexTerms* - Component,formatting,style,styling,insert** *RO-Based Sensor, CAF-Based Sensor, SAF-Based Sensor.*

I. Introduction

The counterfeiting of integrated circuits (ICs) is on the increase, probably impacting the safety of a good type of electronic systems. A counterfeit element is outlined as an electronic half that is not real as a result of it : 1) It is an unauthorized copy; 2) It doesn't change to original element makers style, model, or performance or both; 3) It is not made by the initial element makers or is made by unauthorized contractors; 4) is AN off-specification, defective, or used original element manufacturers' product sold-out as new or working; 5) has incorrect or false markings and/or documentation. The workplace of Technology analysis, a part of the U.S. Department of Commerce, reported over 10,000 incidents involving the marketing of used or defective ICs from 2005 to 2008 alone, the number of reported incidents of used ICs being sold-out as new or remarked as higher grade is far larger than different kinds of counterfeits. It was rumored in this used or defective product thought-about 80%–90% of all counterfeits being oversubscribed worldwide with such estimate on the proportion of used ICs being oversubscribed, and therefore the numbers about semiconductor sales and counterfeiting normally bestowed in, it may well be attainable that the intentional sale of used or defective chips within the semiconductor market may have thought-about regarding $15 billion of all semiconductor sales in 2008 alone. This range may really be a lot of larger as several of the counterfeit ICs go undetected and area unit getting used in systems nowadays. Additionally, from the trends shown in counsel that this range is just about to increase over time. These used or defective ICs enter the market once electronic recyclers divert scrapped circuit boards removed from their selected place of disposal for the needs of removing and reselling the ICs on those boards. As the utilization method sometimes involves a high-temperature atmosphere to get rid of ICs from boards, there are a unit many security problems related to these ICs: 1) a second user IC will act as a ticking time bomb because it doesn't meet the specification of the unused (new) ICs associated 2) an someone will embody extra die on high of the recycled die carrying a back-door attack, sabotaging circuit practicality underneath bound conditions, or inflicting denial of service. Therefore, it's very important that we tend to stop these recycled ICs from coming into essential infrastructures, aerospace, medical, and defense offer chains. In this paper, the term recycled ICs is employed to denote used ICs being sold as new or remarked as higher grades. The terms unused ICs and new ICs represent the ICs that are spanking new. On the opposite hand, most ICs utilized in the sector don't seem to be turned on all the time. Contemplate associate degree IC utilized in a telephone, for example, the telephone could solely be steam-powered on throughout the day for a few amounts. The important (power-on) usage time of the IC would be abundantly shorter than the usage time with power off intervals. In this paper, the term usage time is employed to represent the accumulated power-on time albeit the IC is employed intermittently.

II. DETECTION OF RECYCLED ICs

The major distinction between recycled ICs and unused ICs is that recycled ICs are already used and seasoned aging, as they are off from their original boards and resold in the market. Aging effects, like negative-bias temperature instability (NBTI) and hot-carrier injection (HCI), would have influenced the performance of the recycled ICs because of the modification in threshold voltage.

In this paper two techniques are proposed using light-weight sensors (RO-based and AF-based) to assist with the detection of recycled ICs. RO-based detector is predicated on the aging variations between two ROs to record the usage time of ICs. RO based sensor doesn't need any memory component to store the usage time because it is hidden within the degraded artificial language frequency because of aging. AF-based sensors count the system clock or the shift activity of signals within the style and store the usage time in AF OTP block.

2.1 RO-Based Sensor

Our main objectives in coming up with the RO-based detector are as follows:

1) The detector should age at a high rate to assist sight ICs used for a brief period
2) The detector should expertise no aging or negligible aging throughout producing test
3) The impact of method variations and temperature on RO-based detector should be minimal.
4) The detector should be resilient to attacks.
5) Finally, the live methodologies must be done victimization cheap instrumentality and be in no time and easy.

An embedded RO, these recycled ICs might be known supported its frequency, which can be not up to that of a replacement IC. There are, however, several parameters impacting the frequency of an RO, like temperature and method variations.

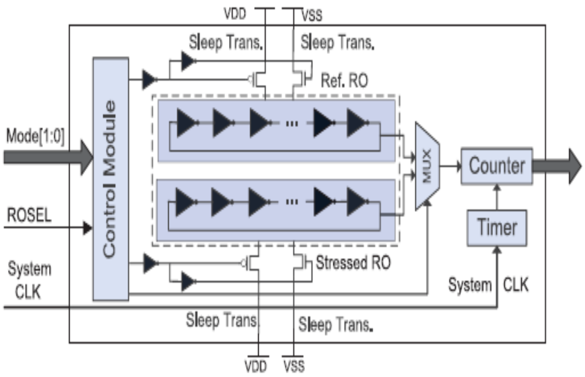


Figure 3.1 Structural Design of RO Based Sensor

RO-based device uses a reference RO and a stressed RO to separate the aging effects from process and environmental variations. The structure of our RO-based device consists of a manner module, a reference RO, a stressed RO, a MUX, a timer, and a counter showing in this figure 3.1. The counter measures the cycle count of the two RO's throughout a prespecified time, which is controlled by the timer. System clock is employed within the timer to attenuate the measuring amount variations due to circuit aging. The electronic device (MUX) selects that RO goes to be measured and is controlled by the ROSEL signal. The reference and stressed ROs unit of measurement identical; every unit of measurement composed of HVT elements.

The inverters in could be replaced by the opposite sorts of gates (NAND, NOR, etc.,) providing they construct an RO. I tend to use smaller stage ROs in our RO-based device considering the counter's measuring speed limits given a technology. For instance, in our 90-nm technology, a 16-bit counter will operate beneath frequency of up to 1 GHz; an inverter-based RO of a minimum of twenty-one stages is then needed.

2.2 i) CAF-Based Sensor

The structure of the CAF-based sensing element that consists of two counters a data read module, an adder, and an AF OTP memory block. Sys_clk within the Figure 3.2 is that the high-frequency system clock, providing clock for various modules as well as the information browse module, the AF block, and registers. Counter1 is employed to divide the high- frequency system clock to a lower frequency signal; Counter2 is employed to live the cycle count of the lower frequency signal.

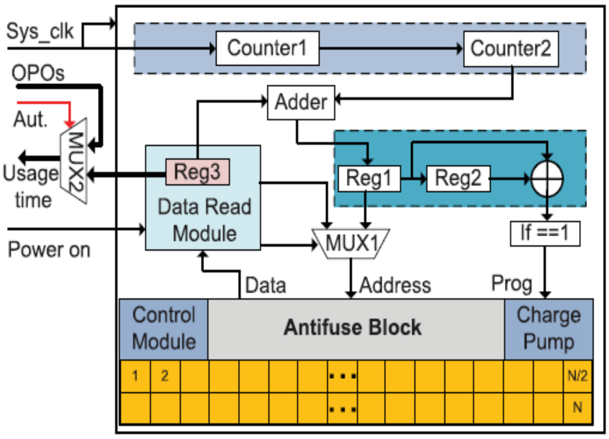


Figure 3.2 Structural Design of CAF Based Sensor

The size of the two counters is adjusted consequently betting on the measurement scale (Ts: the measure reportable by the sensor) and the total activity time (T total). For instance, if Ts is 1 h and T total is one year supporting the specification of an IC, a 38-bit counter1 can meet the need to count the usage time from 20 ns (assume system clock = 50 MHz) to one h and a one4-bit counter2 can count the usage from 1 h to 8760 h (one year). Because the information kept in registers (counters) may well be lost or reset once power provide is off, non eradicable memory is needed during this detector. AN embedded AF OTP block is employed rather than a field-programmable memory board (FPROM) to store the usage time info because of FPROM may well be tampered or altered by attackers. Within the AF block, program is assigned to be one_b1 if the worth in counter2 will increase by 1. Through connecting the output of counter2 to deal with within the AF block directly, the connected AF cell is going to be programmed as one. Therefore, the biggest address of the cell whose content is one are going to be the usage time of CUT supported the activity scale setup by counter1. From the higher than description, the dimensions of the AF block are going to be reduced victimization two counters.

2.2 ii) SAF-Based Sensor

With 2 counters, the area overhead of CAF-based sensor element may still be thought of massive for smaller styles. To scale back the area overhead, we tend to propose SAF-based sensing element supported signals switch activity (SW). Comparing with the structure of SAF-based sensing element showing in the Figure 3.3 is analogous to it of CAF-based sensing element.

The distinction is that CAF-based sensing element counts the cycle of system clock to record the usage time of ICs, whereas SAF-based sensing element counts the switch activity (positive edge) of an explicit variety of nets within the style. With simulations, an explicit variety of nets square measure selected to be the input of a logic gate.

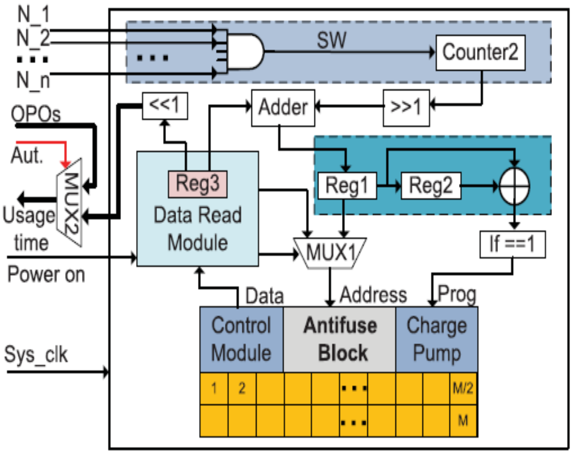
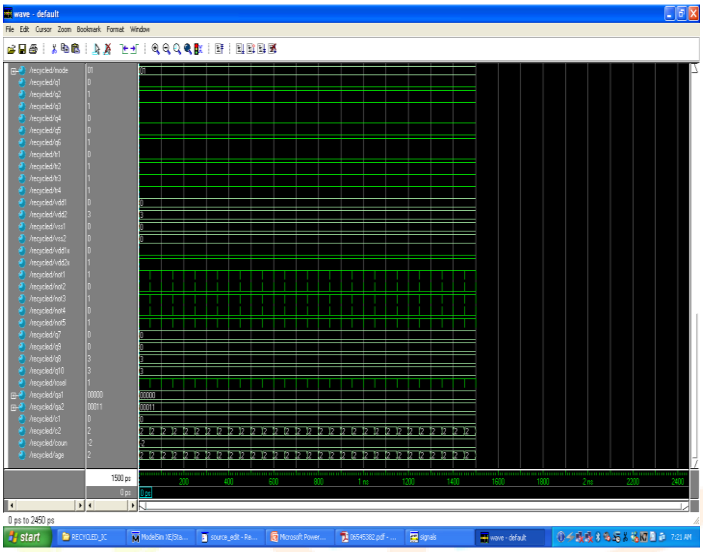


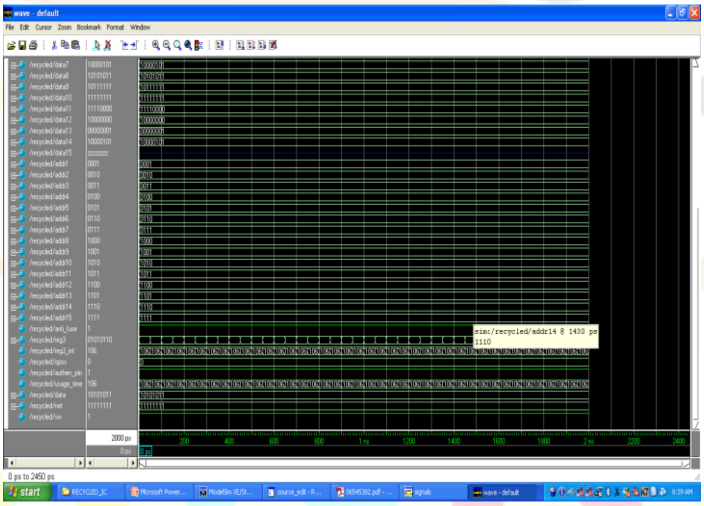
Figure 3.3 Structural Design of SAF Based Sensor

The rule of nets choice is that the switching activity of the output of the AND gate should meet the necessity of the activity scale, as an example if Ts is 1 h, one in all the alternatives may well be four nets with SW(N_1) = 30/60 min, SW(N_2) = 24/60 min, SW(N_3) = 25/60 min, and SW(N_4) = 24/60 min, severally. With completely different practical inputs, the SW, however, may well be considerably completely different. Therefore solely the signals with consistent point beneath completely different inputs area unit chosen after we style a SAF-based detector. From the analysis, internet choice may well be adjusted supported completely different styles and activity scales. Then, the positive pulse of the output of the AND gate (SS signal) are going to be counted by counter2 within the detector.



```
wave - default
/recycled/mode        01
/recycled/q1          0
/recycled/q2          1
/recycled/q3          1
/recycled/q4          0
/recycled/q5          0
/recycled/q6          1
/recycled/tr1         0
/recycled/tr2         1
/recycled/tr3         1
/recycled/tr4         1
/recycled/vdd1        0
/recycled/vdd2        3
/recycled/vss1        0
/recycled/vss2        0
/recycled/vdd1x       0
/recycled/vdd2x       1
/recycled/not1        1
/recycled/not2        0
/recycled/not3        1
/recycled/not4        0
/recycled/not5        1
/recycled/q7          0
/recycled/q9          0
/recycled/q8          3
/recycled/q10         3
/recycled/rosel       1
/recycled/qa1         00000
/recycled/qa2         00011
/recycled/c1          0
/recycled/c2          2
/recycled/coun        -2
/recycled/age         2
1500 ps
0 ps
0 ps to 2450 ps
```

Figure 3.4 Simulation Screenshot of RO Based Sensor



```
wave - default
/recycled/data7        10000101
/recycled/data8        10101011
/recycled/data9        10111111
/recycled/data10       11111111
/recycled/data11       11110000
/recycled/data12       10000000
/recycled/data13       00000001
/recycled/data14       10000101
/recycled/data15       zzzzzzzz
/recycled/addr1        0001
/recycled/addr2        0010
/recycled/addr3        0011
/recycled/addr4        0100
/recycled/addr5        0101
/recycled/addr6        0110
/recycled/addr7        0111
/recycled/addr8        1000
/recycled/addr9        1001
/recycled/addr10       1010
/recycled/addr11       1011
/recycled/addr12       1100
/recycled/addr13       1101
/recycled/addr14       1110
/recycled/addr15       1111
/recycled/anti_fuse    1
/recycled/reg3         01010110
/recycled/reg3_int     106
/recycled/opos         0
/recycled/authen_pin   1
/recycled/usage_time   106
/recycled/data         10101011
/recycled/net          11111111
/recycled/sw           1
2000 ps
0 ps
0 ps to 2450 ps
sim:/recycled/addr14 @ 1430 ps
1110
```

Figure 3.5 Simulation Screenshot of SAF Base

III. CONCLUSION

The Counterfeiting and use of ICs area unit detected victimization low power design that is predicated on 2 techniques victimization lightweight on-chip sensors. Initial technique uses RO based mostly sensing element. During this design is employed to spot the aging victimization reference and therefore the stressed ROs sensing element. Aging is calculated by the frequency distinction between the reference and therefore the stressed ROs sensing element. it's created the simple identification of recycled ICs attainable. Here victimization inverter based ROs sensing element is employed to scale back the quality of the design and conjointly consume less power. It sensing element provides solely associate degree approximation of the usage time in an exceedingly style of aging within the stressed RO.

Second technique uses two different types of AF based sensor. They are CAF and SAF based sensor, the usage time of IC stored in the AF memory using AF based sensors could show how long an IC had been used and antifuse method fused the content are identified in the recycled IC. These techniques provide a more accurate usage time and identify recycled ICs that are only used for a very short period because of the small measurement scale. The area overhead of the CAF based sensor reduced by using SAF based sensor in this method the switching activity only positive edge of a certain number of nets in the design are counted and record the usage time of the ICs. So, the usage time and power are reduced using low power architecture.

In the future using Sequential Optimization Algorithm to efficiently detect the counterfeits and recycled IC for low power applications.

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