IJNRD.ORG ISSN : 2456-4184
INTERNATIONAL JOURNAL OF NOVEL RESEARCH AND DEVELOPMENT (IJNRD) | IJNRD.ORG
An International Open Access, Peer-reviewed, Refereed Journal

Design and Analysis of Two stage CMOS using negative capacitance generation and flipped voltage follower

Neha

MTECH(Microelectronics and VLSI)

Bhagalpur college of Engineering ,Bhagalpur (Bihar)

Bihar Engineering university(BEU),Patna

ABSTRACT: This research paper presents the design and analysis of two stage CMOS structure with enhanced gain-bandwidth product (GBW) , high slew rate and good phase margin. In this paper, the combined use of negative capacitance and Flipped voltage buffer (FVF) proves quite useful for frequency compensation of MOS amplifiers. This method ensures stability without degrading circuit performance at higher frequencies and is well suited for low power and low voltage analog designs . The use of Negative capacitance lowers the parasitic capacitances of the preceding stage and thereby achieves significant improvement in Gain bandwidth product. The flipped voltage follower acts a voltage buffer and exploits pole –zero cancellation technique. The required compensation capacitor is very small so it can save chip area. The workability of the proposed circuit will be verified by using LT SPICE simulation tool with CMOS 0.18µm process parameters.

KEYWORDS: CMOS, Flipped voltage follower, Negative capacitance

INTRODUCTION

Operational amplifiers have become common tools in the electronics industry during the past few years. Many analog and mixed digital signal systems depend on operational amplifiers to function. They are employed in several applications, including filters, amplifiers, and buffers. The CMOS technology has played a significant role in the electronics sector, opening the door for denser and quicker integration. Continuous circuit downscaling lowers power supply requirements and restricts output swing. Although multistage circuits are in considerable demand today, their complexity gives rise to a number of stability problems. Even a two-stage circuit can offer enough gain to satisfy the requirements of wireless transmission, but it has a small bandwidth and inadequate phase margin. With an emphasis on Miller compensation and its variations, numerous compensation approaches are suggested to address this issue. The majority of these techniques make use of the pole splitting approach, which offers stability but results in a smaller gain and bandwidth product. Therefore, a method that improves a circuit's stability while providing enough gain and bandwidth is needed. The research here uses a voltage buffer and negative capacitance to improve a multistage CMOS circuit's slew rate and unity gain frequency.

NEGATIVE CAPACITANCE GENERATION

The negative capacitance compensation method[1] is well-suited for high speed multistage amplifiers. To generate negative capacitance, the Miller effect[8] and an ideal amplifier can be used without any constraint on output or frequency. The MOS stage often uses active load to create large values of load resistance R_L. Assuming that the amplifier drives a parallel combination of R_L and C_L as a load, the bandwidth is then

$$f_{3\text{-dB}} = \frac{1}{2\pi R_L C_L} \qquad (1)$$

where R_L is load resistance and C_L is the parasitic capacitance. The value of C_L can be reduced using a negative capacitance to increase bandwidth. One practical circuit using this concept is shown in Fig. 3.12. The circuit components R_a and C_a exhibit output resistance and parasitic capacitance respectively. These elements also determine the frequency behavior of the circuit. This circuit is meant to cancel some portion of the load capacitance for the amplifying stage plus the input capacitance to the negative capacitance generator (NCG) circuit. The role of capacitance C_N is to link the amplifier's output along with the gain A by making a negative capacitance.

Apparently, after adding the NCG circuit to the output node of the amplifier the bandwidth is extended and given by

$$f_{3-dB} = \frac{1}{2\pi\sqrt{R_a R_L (C_N C_L + C_a C_L + C_N C_a)}} \qquad (2)$$

where C_L is the parasitic capacitance in parallel with R_L . Although a second pole could result from the input capacitance and resistance of the stage, values of R_L sufficient to maximize gain lead to a dominant pole.

FLIPPED VOLTAGE BUFFER

Flipped voltage follower is a high precision buffer. We can also say that flipped voltage follower is a voltage buffer with shunt feedback. Its basic characteristics include low power, low voltage, and low impedance compared to basic source follower. Some of the limitations of source followers are overcome by implementing this circuit.

The condition for the FVF is that the current through QFVF should be held stable, independent of the output current. The low impedance aids the high sourcing at the output node.

$$r_o = \frac{1}{g_{mFVF} g_{m1} r_{oFVF}} \qquad (3)$$

Here, gmFVF and gm1 are the transconductances of QFVF and Q1 respectively, and roFVF is the output resistance of transistor QFVF. The value of roFVF is in the order of 20– 100Ω. Note that Q1 provides shunt feedback and that QFVF and Q1 form a two pole negative feedback loop. The output impedance of the control transistor is minimized by the feedback loop.

OP – AMP DESIGN AND IMPLEMENTATION

The proposed circuit makes use of two frequency compensation approaches as negative capacitance and voltage buffer. The transistor level implementation is given in Fig.2. It can be seen that there are two gain stages connected in series and a voltage buffer with compensation capacitor C_C is connected between nodes A and B. The first stage consist of NMOS M1 and M2 forming a differential amplifier with PMOS M3–M4 realizing a current mirror as an active load. Transistors M7–M9 are arranged in a way to generate a negative capacitance and provide small gain [1]. The FVF cell is acting as a voltage buffer and realized by means of transistors M10–M12. This cell offers more linearity and high speed to the circuit. The compensation capacitor $C_C$helps to improvise the phase margin of circuit where as the feedback capacitance C_N is accountable for bandwidth. Since the first stage uses an active load of high output resistance so it provides most of the gain of the circuit. The NCG circuit aids to maximize zero of the circuit's transfer function and thereby increases GBW. The output stage is a common source amplifier and consists of PMOS M5 and NMOS M6. The first stage is loaded with NCG which is generating a negative capacitance and thereby lowering the effect of first stage parasitic capacitance. The final stage is common source amplifier and possesses output resistance r_{o2}, transconductance g_{m2} and total equivalent load capacitance C_L. The voltage buffer (FVF cell) compensation network is connected between two nodes A and B. The output impedance of this buffer is expressed as r_{ob}.

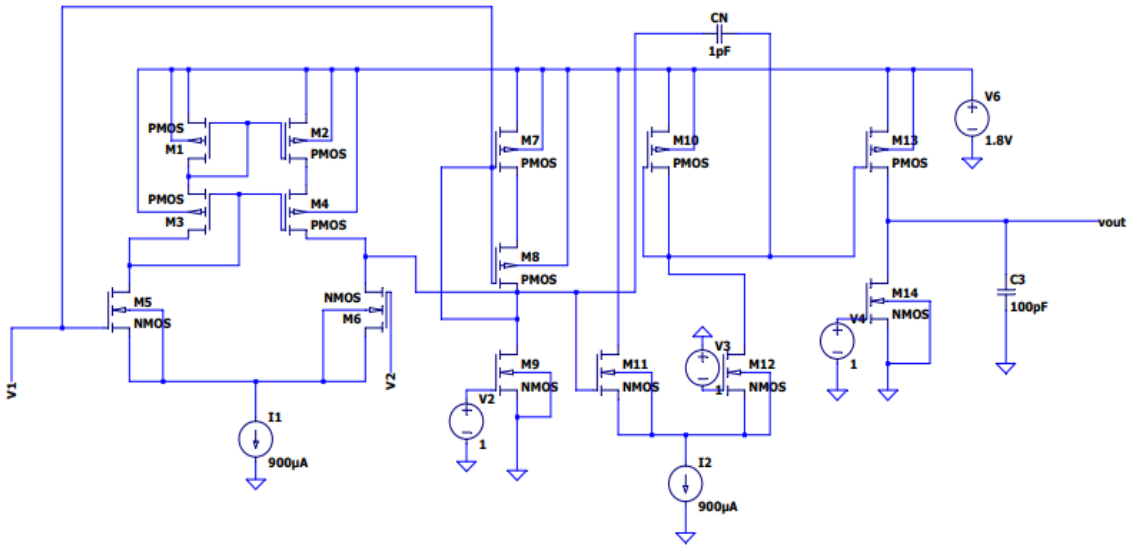

FIG 1. Two stage OP-AMP without using compensation capacitor

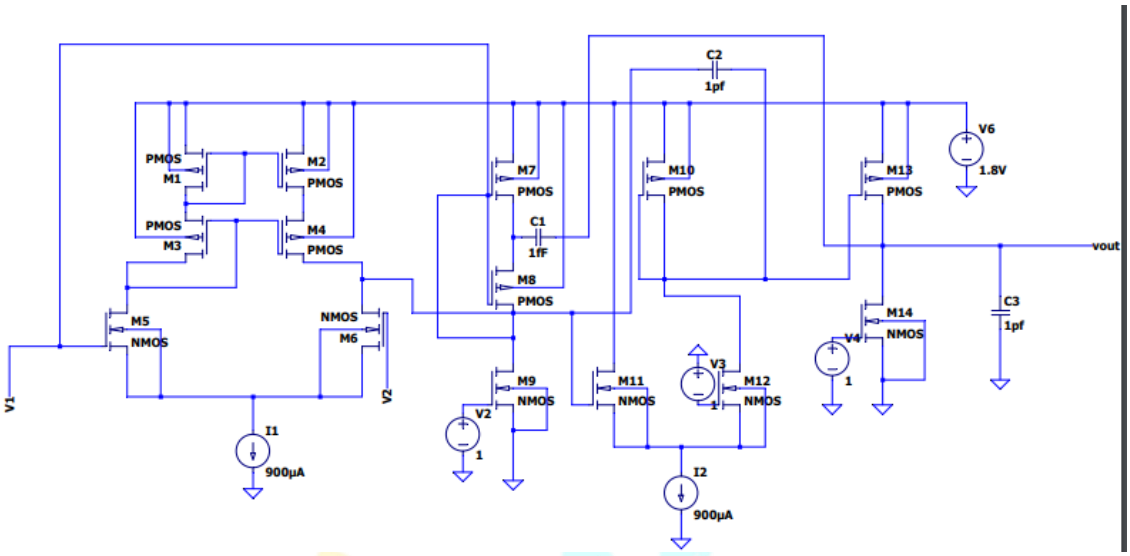

FIG2. Two stage OP-AMP using compensation capacitor

TABLE1. SPECIFICATION OF TWO STAGE OP-AMP DESIGN

Specification name	Value
1. Technology	0.18μm
2. Power supply	1.8V
3. DC bias current	900 μA
4. Aspect ratio	(M1, M2)= 56/1 (M3, M4, M9 , M11, M12,M14) = 70/1 (M7, M8, M10) = 40/1 M13 = 20/1
5.Compensation capacitor (C_C)	1Ff
6. Load capacitance (C_L)	100 Pf
7.Negative capacitance (C_N)	0.1 Pf

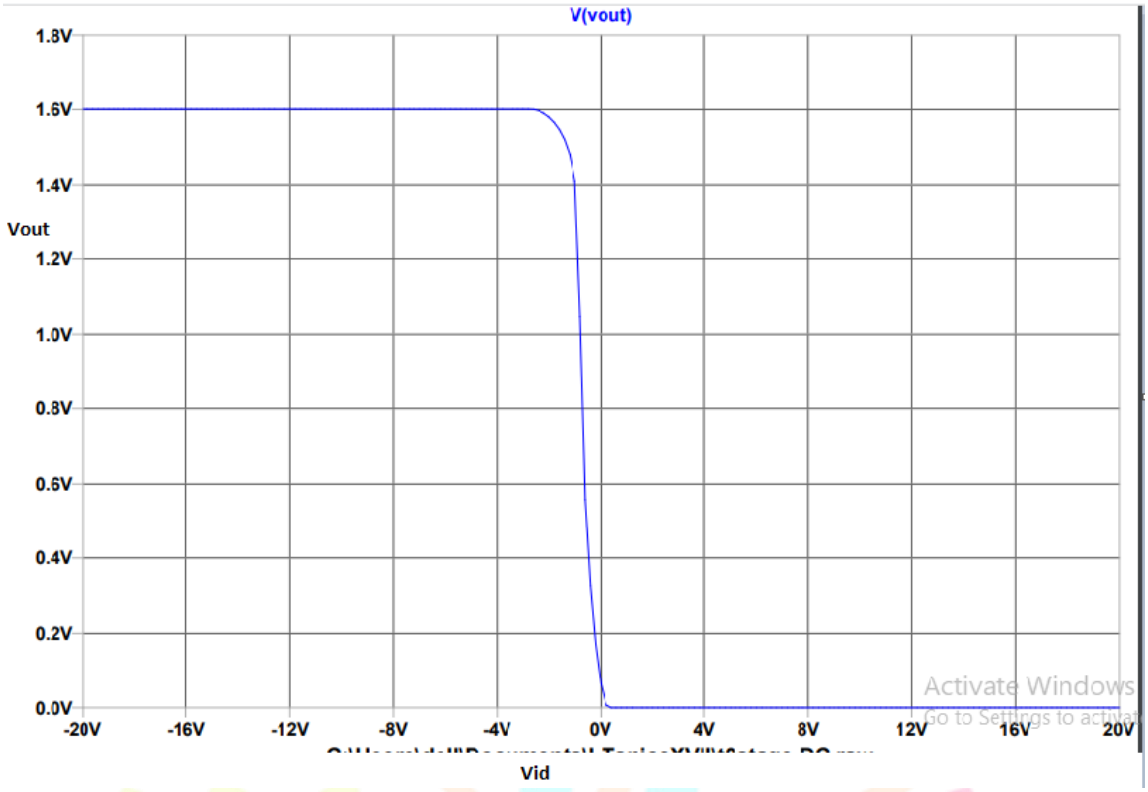

FIG3. DC Response of the two stage op amp

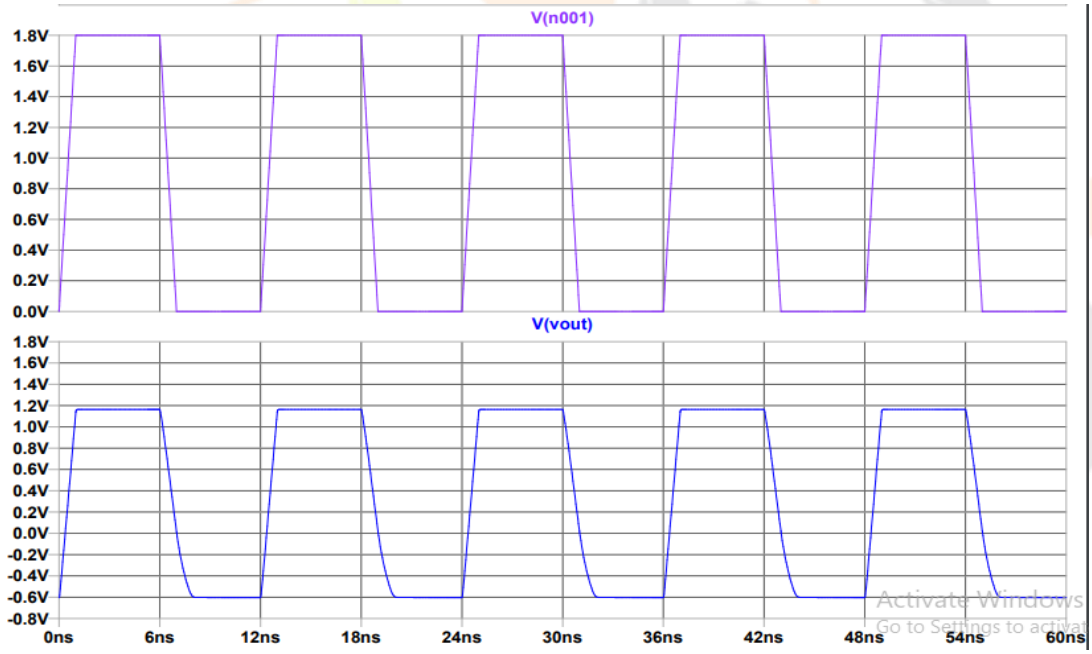

FIG4. Transient response of two stage opa amp.

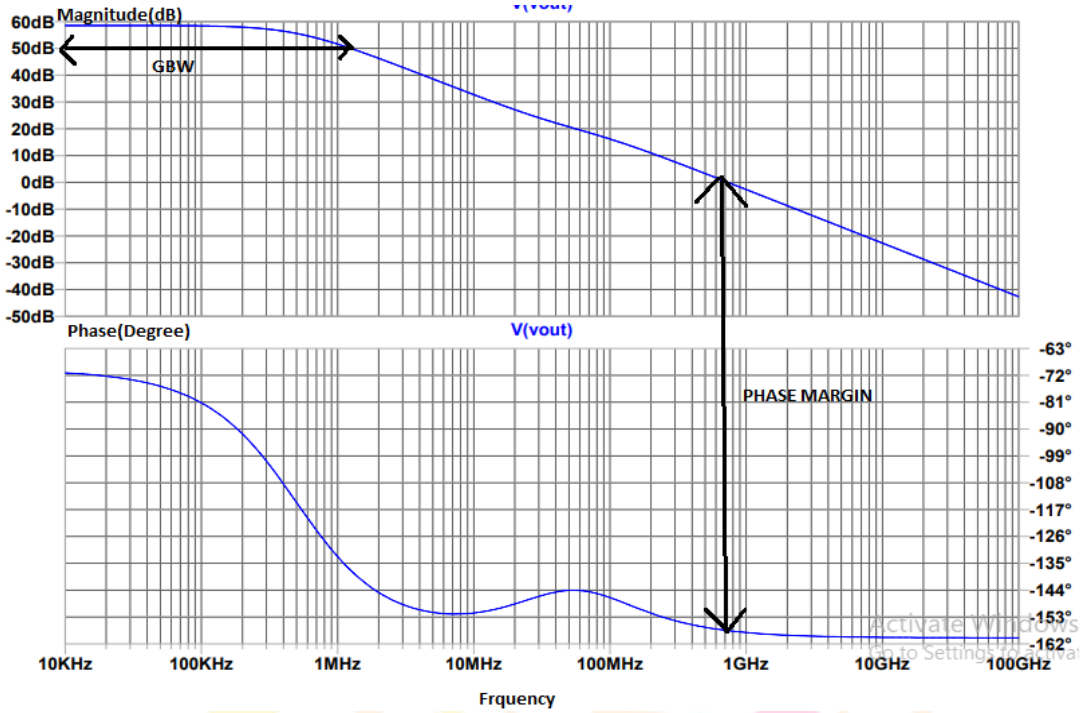

Fig 5.Gain and phase response of uncompensated circuit

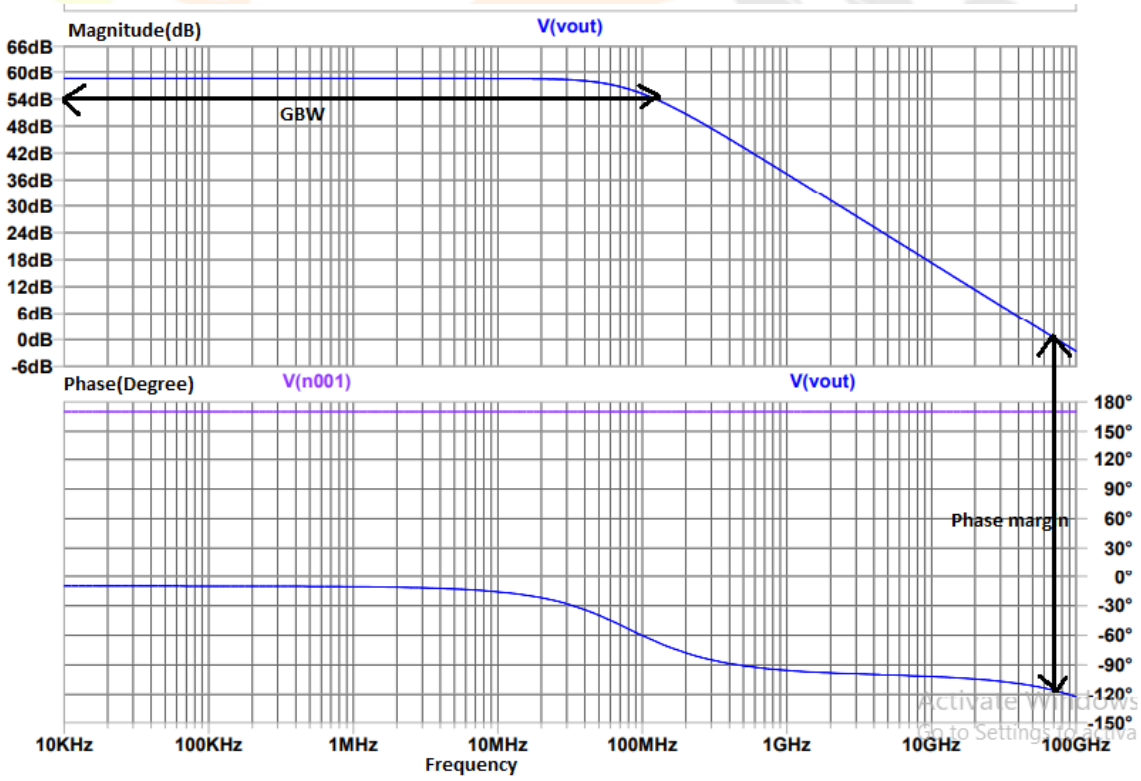

FIG 6. Gain and phase response of compensated circuit

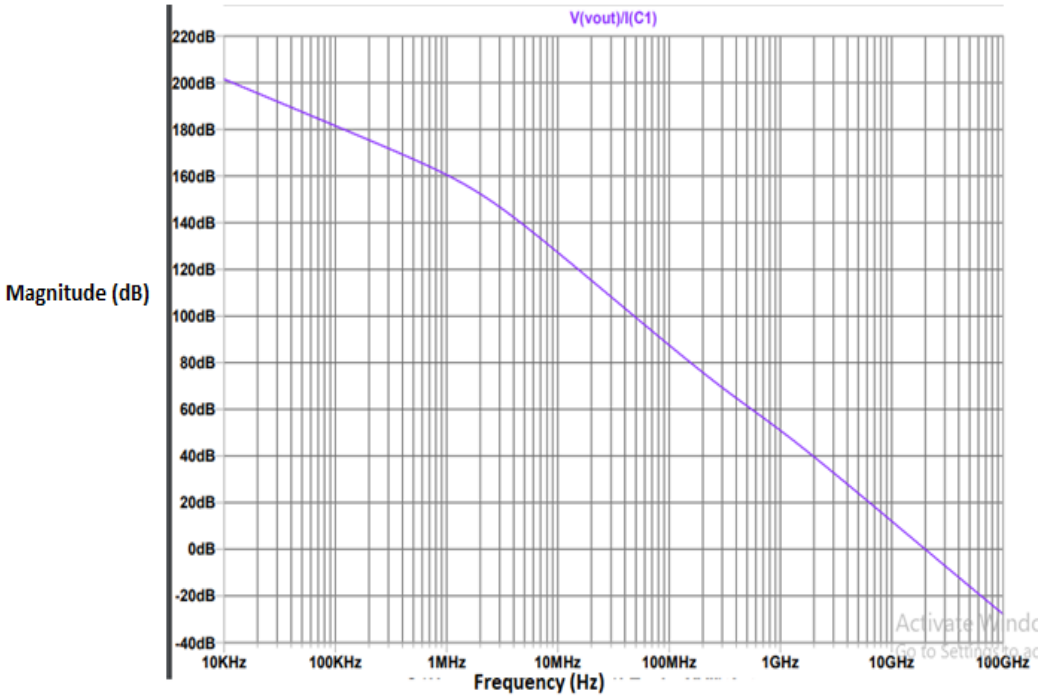

FIG7. Output impedance of the two stage op amp

Table 2 Simulated result for typical conditions

Parameter	**Value**
Gain	59 dB
Gain product product	59.18 GHz
Phase margin	64º
Slew rate	83.13 V/µs

CONCLUSION

The work proposed here presents a method to frequency compensate a two stage CMOS circuit using negative capacitance and FVF. The transistor level circuit given in Fig. 2 has been simulated by using LT spice simulation tool with TSMC CMOS 0.18 lm process parameters. The maximum bias current in the circuit is 0.9 mA and supply voltage is set to 1.8 V. All transistors are working in saturation mode . The slew rate of proposed circuit is high as the output voltage of the given circuit changes rapidly with respect to time. The simulated transient response with a 1 pF load and slew rate measured is 83.13 V/µs . The AC analysis results with suggested method

are depicted in Fig. 4.8. The gain bandwidth product (GBW) is 59 GHz, phase margin (PM) is 64º. In case when no compensation is used the circuit is the phase margin (PM) is 27º .The load conditions are kept same for both the cases. These simulation results make it obvious that using proposed technique GBW, PM and GM can be greatly improved. Input–output characteristics are revealed in Fig. 5 and 6 It clearly show signs of high linearity and enhanced stability of proposed circuit. Figure 7 plots the variation in output impedance with respect to frequency. From Fig.7, it can be confirmed that the output impedance (Rout) of the proposed circuit decreases at a fast rate at higher frequencies. It can be checked from Fig. 7 that at 100 MHz output impedance is 88 dB and at 1 GHz it is 51 dB. The bandwidth of a circuit can be modified by using an impedance element between input and output as decrease of Rout in high frequency region results into larger current at the output.

REFERENCES

1. Genz, Adrian PC. *Operational Amplifier Bandwidth Extension Using Negative Capacitance Generation*. Brigham Young University, 2006.

2. Mahattanakul, Jirayuth. "Design procedure for two-stage CMOS operational amplifiers employing current buffer." *IEEE Transactions on Circuits and Systems II: Express Briefs* 52, no. 11 (2005): 766-770.IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 52, NO. 8, AUGUST 2005

3. Mahattanakul, Jirayuth, and Jamorn Chutichatuporn. "Design procedure for two-stage CMOS opamp with flexible noise-power balancing scheme." *IEEE Transactions on Circuits and Systems I: Regular Papers* 52, no. 8 (2005): 1508-1514.

4. Ahuja, Bhupendra K. "An improved frequency compensation technique for CMOS operational amplifiers." *IEEE journal of solid-state circuits* 18, no. 6 (1983): 629-633.

5. Bandyopadhyay, Sayan, Deep Mukherjee, and Rajdeep Chatterjee. "Design of two stage cmos operational amplifier in 180nm technology with low power and high cmrr." *Int. J. of Recent Trends in Engineering & Technology* 11 (2014).

6. Sadeqi, Abolfazl, Javad Rahmani, Saeed Habibifar, Muhammad Ammar Khan, and Hafiz Mudassir Munir. "Design method for two-Stage CMOS operational amplifier applying load/miller capacitor compensation." (2020): 153-162.

7. Goyal, Shilpa, Nitin Sachdeva, and Tarun Sachdeva. "Analysis and design of a two stage cmos op-amp with 180nm using miller compensation technique." *International Journal on Recent and Innovation Trends in Computing and Communication* 3, no. 4 (2015): 2255-2260.