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Analysis of Domino logic based full adder using Mentor Graphics

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ABSTRACT

Designing a circuit with low power, high speed performance is one of the challenging aspects. Since most recent VLSI devices are becoming portable, area-efficient devices are the most commonly utilized type. As the number of transistors will increase, correspondingly area, delay and power consumption of the device will also increase. Therefore, a technology is required by which the area can be reduced and increase the performance of the device. A fundamental component of multiplexer and processor designs is the full adder. It is possible to implement full adders with CMOS technology. A major factor influencing the CPU performance on VLSI circuit chips is the CMOS technology. In this project, implemented various full adder circuits using CMOS technology such as Standard Full adder circuit, Low Power Hybrid Full Adder, Full Adder Circuit using Modernized Full Sway Ex-or, Ex-nor gates and Domino logic based Full adder circuit. The analysis includes examining key parameters such as propagation delay, power consumption, and signal integrity. Findings from this analysis contribute to the enhancement of full adder designs, offering insights into potential optimizations and trade-offs. This project explores the design and performance analysis of a full adder circuit using Mentor Graphics tools.

1. INTRODUCTION

The importance of a full adder lies in its role as a fundamental building block in digital circuits, particularly in binary arithmetic operations. Full adders are integral components of ALUs, which are crucial parts of microprocessors and digital processors. It can perform addition on three binary inputs: A, B, and carry input (Cin).). And produces a sum(S) and a carry output (Cout). In early days of electronic computing, full adders were implemented using discrete components like vacuum tubes and later with transistors which were bulky, power consuming, and limited in terms of speed. As semiconductor industry advanced, CMOS technology became widely

adopted for digital circuits, including full adders, due to its low power consumption and improved noise margins. Since many FA (full adder) topologies have been presented, particularly in the recent past, it is imperative to assess their performance metrics on a shared platform so that VLSI designers can select the most appropriate FA (full adder) architecture for their system needs. Power dissipation was less of an issue after the invention of the transistor and the IC (Integrated Circuit) several decades later. As a result, as demonstrated by general-purpose microprocessors, the amount of power per unit area has continued to increase and the related issue of heat removal and cooling has continued to worsen.

2. ITERATURE REVIEW

1)Kamlesh Kukreti, Prashant Kumar, Shivangi Barthwal, Amit Juyal, Alankrita Joshi, "Performance Analysis of Full Adder based on Domino Logic Technique". Sixth International Conference on Inventive Computation Technologies Proceedings [ICICT 2021] Part number CFP21F70-ART for IEEE Xplore. Domino logic gives us very accurate results with a smaller number of transistors and minimum delay as compare to the CMOS design logic.

2)Rahul Mani Upadhyaya, R.K.Chauhana and Manish Kumara, "Performance Evaluation of Efficient Low Power 1-bit Hybrid Full Adder", ADCAIJ: Advances in Distributed Computing and Artificial Intelligence Journal Regular Issue, Vol. 11 N. 4 (2022). This research states that the average power dissipation of 12.56nW and area occupied by the circuit is also get reduced.

3) Design a Full Adder Circuit using Modernized Full Sway Exclusive-Or and Exclusive-Nor Gates in by Venkatan Yashwanth Goduguluri, Guntupalli Sai Divya Madhuri, Balusupati Bhanu Pranavi, Bhimineni Kalyani, and Annam Sai Anusha in 130nm Mentor Graphics", International Journal of Innovative Technology and Exploring Engineering (IJITEE) , January 2020. This proposed circuit eliminates the voltage sway quandary in the previously existed EX-OR and EX-NOR design

4)Saurabh J Shewale and Sonal A Shirsath, "Design and Analysis of CMOS Full Adder", International Journal of Advanced Research in Science, Communication and Technology (IJARSCT) Volume 9, Issue 1, September 2021.

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3. PROPOSED METHODLOGY

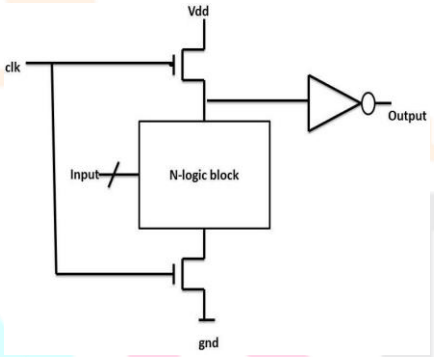


Fig 3.1 Domino Logic

Transistor density in the rapidly expanding VLSI sector is rising daily at a rapid rate. Transistor density will double every 18 months in accordance with Moore's law. As the number of transistors will increase, correspondingly area, delay and power consumption of the device will also increase. Therefore, a technology that reduces the area and boosts the device's performance is needed. From the past few decades CMOS technology is being used

for designing the chips in semiconductor industry, but as the number of transistors are increasing, area of the device and delay both are increasing. So, it requires to switch to a technology, which uses lesser area and smaller delay. Therefore, the one-bit full adder is designed using Domino logic, and different performance parameters like as area, latency, and power consumption are evaluated between the two technologies.

CMOS Logic- CMOS is abbreviation of "Complement Metal Oxide Semiconductor". CMOS logic uses the *p*-MOS and *n*omos transistors as shown in Fig 1.1, and they work as a pull up and a pull-down transistor respectively. When input will be low then *p*-MOS will be on and it will charge the output node to Ved, and when input will be high *n*-MOS will turn on and charge stored at the output node get a conducting path between output node and ground. CMOS logic design has various numbers of advantages as compare to the others logics which were used before. In this both the transistors are connected in complementary form i.e., Transistors work in pairs; when one is on, the other is off.

4.
ESIGN OF DOMINO LOGIC FULL ADDER

Domino logic- Domino logic family find a wide variety of application, where less transistor count and high speed of operation such as microprocessor, dynamic memory, digital signal processors are required. A development of CMOS-based dynamic logic approaches, Domino logic use either p-MOS or n-MOS for the pull-up or pull-down network. The methodology of designing full adder by using Domino logic employees' lesser number of transistors as if compared to conventional CMOS logic and provides high performance device.

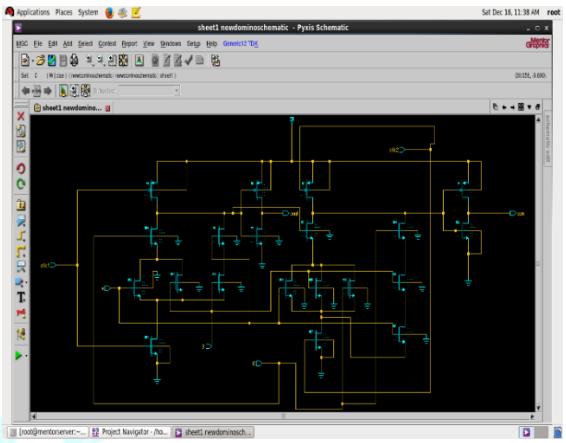
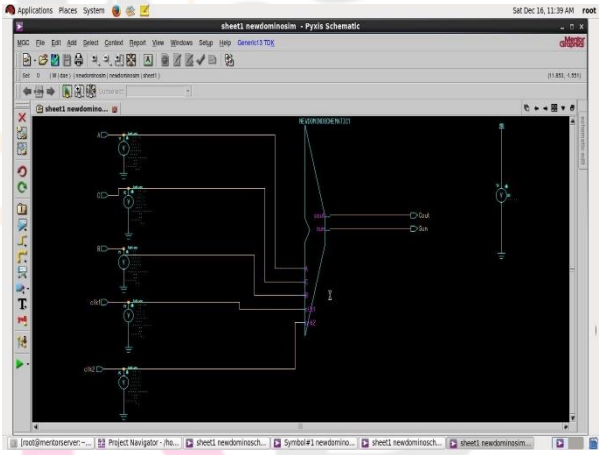


Fig 4.1 Schematic design of domino logic based full adder.

Designing of one- bit full adder based on CMOS logic- The one- bit full adder schematic using CMOS logic is shown in fig 2.6. This circuit uses the 14 p-MOS transistors which are used for charging the output capacitance and 14 n-MOS



transistors for discharging the output node according to value of inputs.

Domino logic has gained significant attention in recent years due to its ability to achieve high-speed operation and reduced power consumption in digital circuit design. In this paper, we propose a domino logic-based full adder design tailored for 130nm technology nodes. The simulation results demonstrate the effectiveness of the domino logic-based full adder design in achieving reduced delay

and area occupancy. With only 20 transistors, the design achieves a delay of 29.85ns, meeting the high-speed requirements of modern integrated circuits. Furthermore, the design exhibits a 28% decrease in area occupancy compared to conventional full adders with 28 transistors, highlighting its improved resource utilization and area efficiency. These results underscore the potential of domino logic-based circuits for optimizing both performance and area in digital circuit design. These findings demonstrate the potential of domino logic-based circuits for addressing the challenges of modern integrated circuit design, paving the way for the development of faster and more compact arithmetic units in digital systems. Future research directions may explore further optimizations and extensions to advance the state-of-the-art in domino logic-based circuit design methodologies.

Fig 4.2 Simulation of Domino logic based full adder

Domino logic has gained significant attention in recent years due to its ability to achieve high-speed operation and reduced power consumption in digital circuit design. In this paper, we propose a domino logic-based full adder design tailored for 130nm technology nodes. The simulation results demonstrate the effectiveness of the domino logic-based full adder design in achieving reduced delay and area occupancy. With only 20 transistors, the design achieves a delay of 29.85ns, meeting the high-speed requirements of modern integrated circuits. Furthermore, the design exhibits a 28% decrease in area occupancy compared to conventional full adders with 28 transistors, highlighting its improved resource utilization and area efficiency.

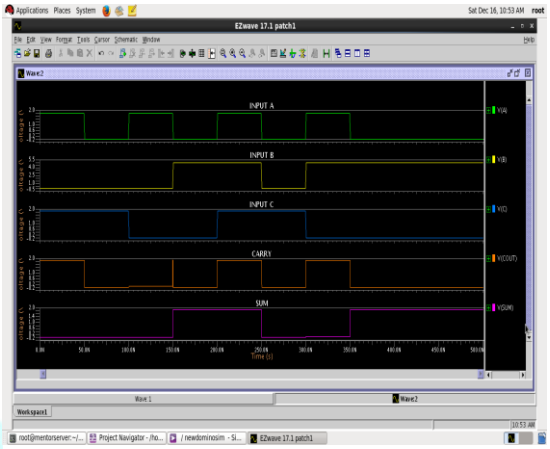


Fig 4.3 Simulation results of Domino logic based full adder

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5. COMPARISON OF VARIOUS PARAMETERS OF DOMINO LOCIC FULL ADDER WITH OTHER FULL ADDERS

Comparing the performance of different full adder implementations based on transistor count and delay time in a 130nm technology node reveals interesting insights. The standard full adder with 28 transistors, despite being a common implementation, has a relatively high delay of 50.076ns. This delay is primarily due to the larger

number of transistors involved, which increases the propagation time through the circuit.

The hybrid full adder, boasting a reduced transistor count of 14, demonstrates a notable improvement in delay time, clocking in at 45.886ns. The reduced transistor count suggests a simplified design, contributing to the faster operation compared to the standard full adder.

However, it still falls short in terms of delay when compared to more modernized approaches. The modernized Sway full adder, incorporating 18 transistors, shows a slightly better delay performance of 49.99ns compared to the standard full adder. This indicates some optimization in the design, likely leveraging advancements in circuit techniques to reduce delay while maintaining a reasonable transistor count. However, the standout performer in terms of speed is the domino logic-based full adder, despite having 20 transistors. With a delay of only 28.985ns, significantly lower than the other implementations mentioned, it showcases the effectiveness of domino logic in speeding up arithmetic circuits. The domino logic approach, characterized by its pipelined operation and efficient use of transistors, allows for faster switching times and reduced delays compared to traditional static logic implementations.

NAME OF THE PARAMETER	STANDARD FULL ADDER	HYBRID FULL ADDER	ONE-BIT FULL ADDER USING MODERNIZED FULL SWAY USING EX-OR AND EX-NOR	DOMINO LOGIC BASED FULL ADDER
TRANSISTORS COURNT	28	14	18	20
AREA (DECREASED %)	0	50	35	28

TECHNOLOGY	130nm	130nm	130nm	130nm
DELAY	50.076Ns	45.886Ns	49.998Ns	28.845Ns

Table 5.1 Comparison table

6. REFERENCES

1. Kamlesh Kukreti, Prashant Kumar, Shivangi Barthwal, Amit Juyal, Alankrita Joshi, "Performance Analysis of Full Adder based on Domino Logic Technique". Sixth International Conference on Inventive Computation Technologies Proceedings [ICICT 2021] Part number CFP21F70-ART for IEEE Xplore.
2. Rahul Mani Upadhyaya, R.K.Chauhana and Manish Kumara, "Performance Evaluation of Efficient Low Power 1-bit Hybrid Full Adder", ADCAIJ: Advances in Distributed Computing and Artificial Intelligence Journal Regular Issue, Vol. 11 N. 4 (2022).
3. Using modernized Full Sway Exclusive-Or and Exclusive-Nor Gates, Venkatan Yashwanth Goduguluri, Guntupalli Sai Divya Madhuri, Balusupati Bhanu Pranavi, Bhimineni Kalyani, and Annam Sai Anusha designed a full adder circuit.
January 2020 issue of International Journal of Innovative Technology and Exploring Engineering (IJITEE), "in 130nm Mentor Graphics"
4. Saurabh J Shewale and Sonal Shirsath,

"CMOS Full Adder Design Analysis," International Journal of Advanced Research in Science, Communication, and Technology (IJARSCT), September 2021, Volume 9, Issue 1. A comparison of complementary MOSFET (CMOS) complete adder circuits is presented in this research.