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A REVIEW ON DESIGN AND ANALYSIS OF SEQUENTIAL CIRCUITS USING LOW POWER ADIABATIC TECHNIQUES

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ABSTRACT: Power consumption in a circuit has been a major problem in the usage of devices and leads to serious issues of over battery or supply drain. Reducing power consumption in real-world applications is crucial for battery life and thermal management in electronic devices. This paper proposes a logic-independent approach to achieve power reduction in sequential circuits, a fundamental building block in digital systems. We look forward to use the power reduction techniques. we use the adiabatic logic principle so as to reduce the power consumption across a circuit so as to reduce the power dissipation in a device. The energy recovery reduces the power consumption and reuses the energy through reversible logic. The aim of study is to design and implement sequential circuits using such adiabatic techniques using TANNER TOOLS software.

KEY WORDS: Very large-scale integration **(**VLSI), complementary metal-oxide semi- conductor (CMOS), p-channel metal-oxide semiconductor (PMOS), n-channel metal-oxide semiconductor (NMOS), positive feedback adiabatic logic (PFAL), efficient charge recovery logic (ECRL), simulation program with integrated circuit emphasis (SPICE)

1. INTRODUCTION

Sequential circuits are fundamental building blocks in digital electronics, playing a crucial role in storing and processing information over time. Unlike combinational circuits, which produce an output solely based on the current input, sequential circuits incorporate memory elements to retain information about past inputs. This ability to "remember" past states enables sequential circuits to exhibit dynamic behaviour, making them indispensable in applications requiring sequential logic, such as digital counters, shift registers, and finite state machines.

some of the examples of sequential circuits are latches, flipflops, registers, counters etc.so here we implemented sequential circuits using the above adiabatic techniques and analysed the results

A. FLIPFLOP

Flip-flops are single-bit memory elements with two stable states (typically represented as O and 1). They can be triggered by clock signals to switch states. Common types include SR, D, JK, and T flip-flops. Master-slave configurations are also used.

The paper specifically discusses D flip-flops, which store data based on the clock input. When the clock is high, the data input is captured at the output. When low, the output retains its previous value. These are the simplest flipflops which are used as basic building blocks for many other circuits. General D-flipflop circuit is given below

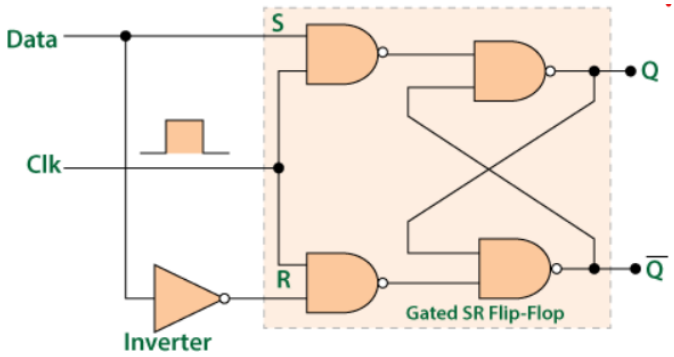

FIG.1 Basic D flipflop circuit

Table.1 Truth table for D-flipflop

D	Q(Current state)	Q(n+1) (next state)
0	0	0
0	1	0
1	0	1
1	1	1

B. REGISTERS

Registers are formed by connecting multiple flip-flops, enabling storage and shifting of data according to specific needs. They can be configured for serial or parallel input/output operations (SISO, SIPO, PISO, PIPO)..

SIPO (Serial in Parallel Out): It is a type of shift register in which data inputs of flipflops are connected in series and the output are taken parallel

A 3-bit SIPO register example is presented, where data enters serially and outputs are available in parallel.

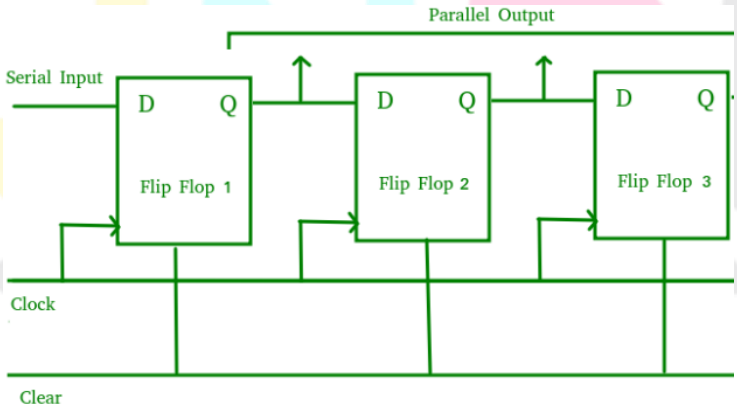

FIG.2 3-bit SIPO register circuit

1.1 CMOS METHOD

Cmos (complementary metal oxide semiconductor) is one of technology of designing an integrated circuit which has low power dissipation and is a traditional technique which is still in use. It uses combination of both NMOS (N- channel MOSFET) and PMOS (P- channel MOSFET). The basic structure of Cmos is given below

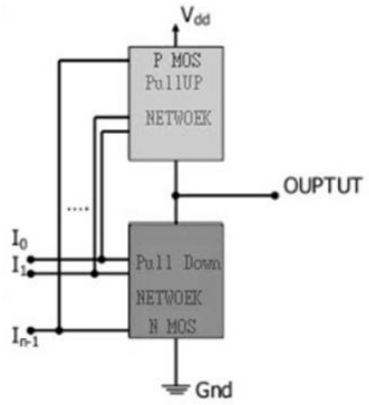

FIG.3 Basic structure of CMOS circuit

Cmos has two types of network, pull-up network and pull-down network. In pull-up network only PMOS are present and in pull-down network only NMOS are present. Inputs are given to both pull-up and pull-down network. The PMOS will conduct when the given input is low and the NMOS will conduct when the given input is high. Based on inputs the working of pull-up and pull-down network changes.

D-FLIPFLOP Using Conventional CMOS

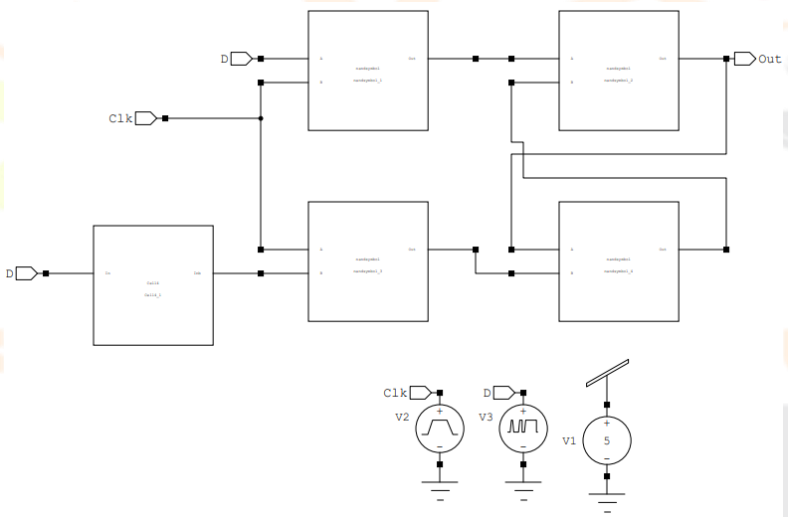

FIG.4 CMOS D-flipflop circuit

The above D-flipflop is designed using cmos nand gate symbol and, the flipflop is made into a symbol for further use.

3-BIT SIPO REGISTER USING CONVENTIONAL CMOS

In the below figure 3-bit SIPO register is designed using 3 CMOS D-Flipflops

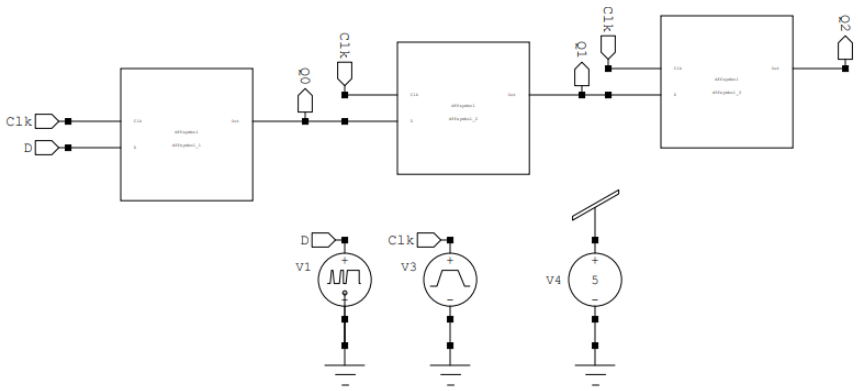

FIG.5 3-bit CMOS SIPO register circuit

2. LOW POWER ADIABATIC TECHNIQUES

The term adiabatic refers to isolation with environment i.e. excluding the loss of energy with environment. Here adiabatic techniques refer to the loss of power in circuit without considering the external losses i.e. environment related power loss. Adiabatic techniques use reversible logic to save power while the process of charging and discharging is going on in the circuit. It has two phases one is pre-charge and other is charge recovery. Pre-charge phase is before delivery of energy and charge recovery phase is at recovery of the energy. Adiabatic techniques have two types they are fully adiabatic and quasi (or) partial adiabatic based on recovery of charge. When it recovers only some part of charge then it is partial (or) quasi if recovers completely then it is fully adiabatic. Fully adiabatic techniques are very complex to design and implement so here we are using quasi adiabatic techniques in this paper. Some examples of quasi adiabatic techniques are PFAL, ECRL, 2N-2N2P, CAL, NERL, etc.

2.1 **PROPOSED PFAL LOGIC**

In this paper we proposed an adiabatic technique PFAL which stands for Positive Feedback Adiabatic Logic. It is an adiabatic technique which has been developed as an alternative to CMOS for the purpose of power reduction . The basic circuit of PFAL circuit is given below

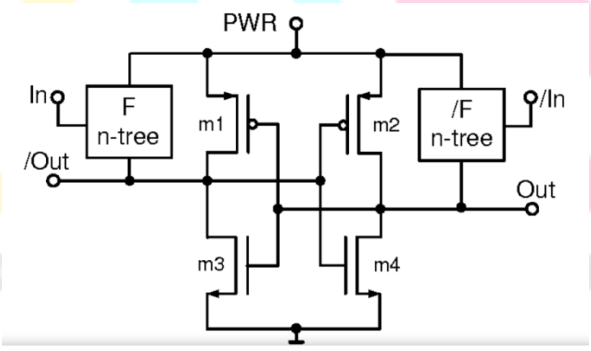

FIG.6 PFAL Basic structure

It is an adiabatic technique which uses dual railing for partial recovery of energy. The main block of PFAL is amplifier latch consists of two PMOS and two NMOS transistors. They act as feedback and responsible for reducing power consumption. And a complementary function blocks is also parallel with two PMOS devices of the latch. The complementary function blocks represent the pull-down network and complementary pull-down network. Here the pull-down network is connected parallel to the PMOS. When state transition occurs the positive feedback present in the circuit amplifies the change and ensures a clear logic state

D-FLIPFLOP Using PFAL

Simply we replace the NAND in basic d-flipflop circuit with PFAL NAND then we will get the flipflop implemented using PFAL technique.

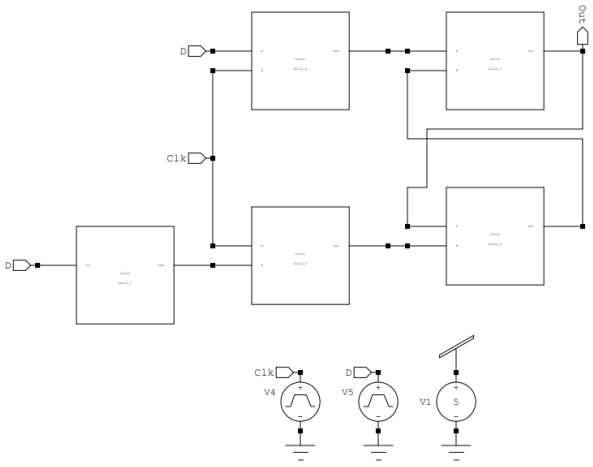

FIG.7 PFAL D-flipflop circuit

3-BIT SIPO REGISTER USING PFAL

The 3-bit serial in parallel out register is implemented using 3 PFAL D-flipflops as shown in the below figure

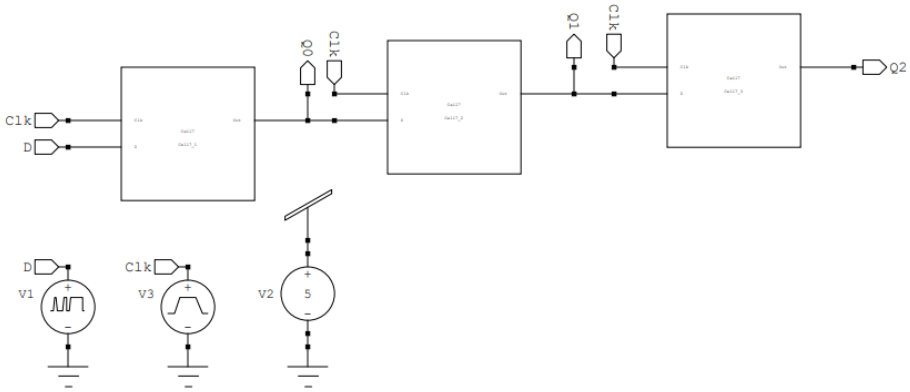

FIG.8 3-bit PFAL SIPO register circuit

2.2 PROPOSED ECRL LOGIC

In this paper we also proposed another adiabatic technique ECRL stands for Efficient Charge Recovery Logic.it also developed as an alternative to CMOS for reducing the power consumption. The basic ECRL circuit is as shown in figure

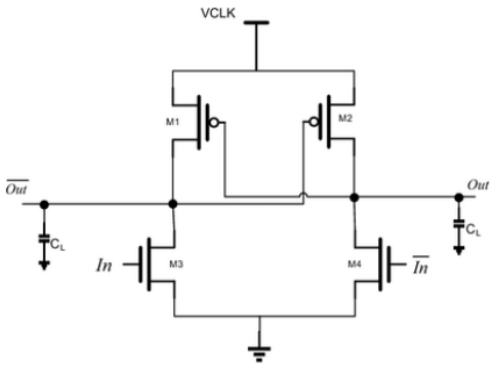

FIG.9 ECRL basic structure

It comprises of two cross-coupled and two PMOS devices and complementary functional blocks are connected to the PMOS. ECRL minimizes the energy dissipation while switching between the states. Unlike CMOS, ECRL reduces the energy dissipation in form of heat and reuses the energy by storing the energy in a capacitor. ECRL has a charging discharging approach for charge recovery, the power supply voltage changes along with logic transitions which minimizes energy waste.

D-FLIPFLOP Using ECRL

Here we simply replace the normal CMOS NAND gates in the flipflop circuit with ECRL NAND circuits then we get the flipflop implemented with ECRL technique. The circuit diagram is given below

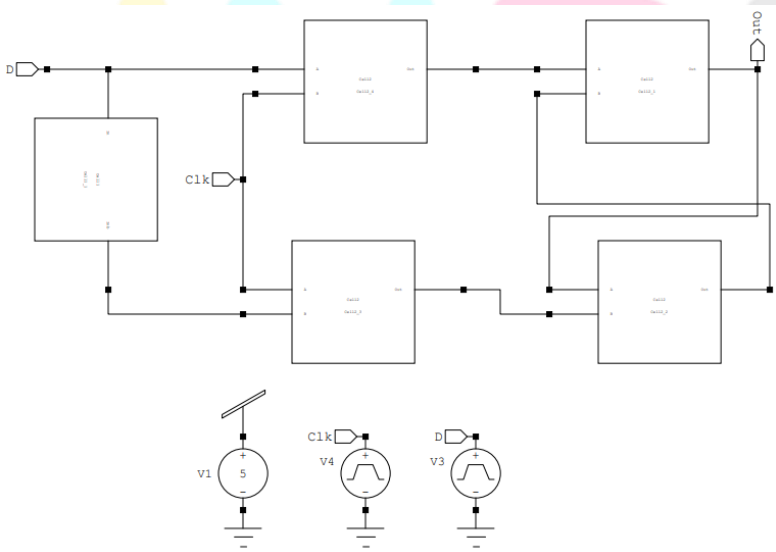

FIG.10 ECRL D-flipflop circuit

3-BIT SIPO REGISTER USING ECRL

The 3-bit serial in parallel out register is implemented using 3 ECRL D-flipflops as shown in the figure

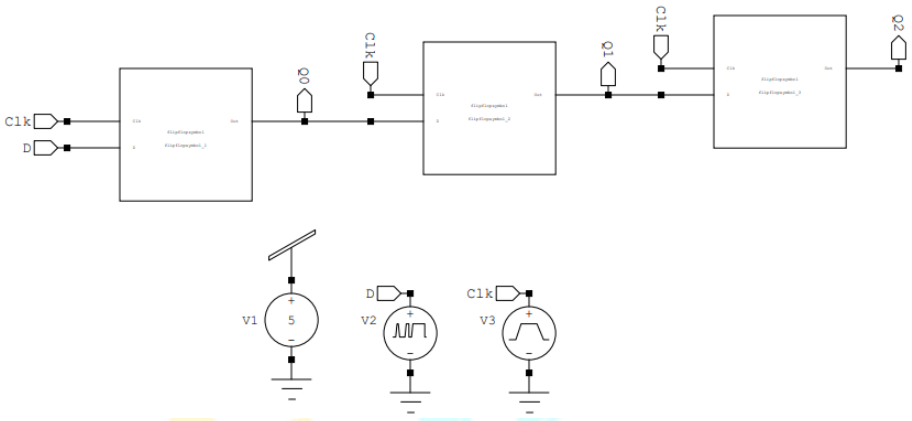

FIG.11 3-bit ECRL SIPO register circuit

3. SIMULATION RESULTS AND DISCUSSIONS

D-flipflop and 3-bit SIPO register are implemented using PFAL and ECRL techniques. Their power consumption is calculated and compared in below tables

Table.2 Power analysis of D-flipflop

CIRCUIT	PFAL	ECRL	CMOS
D-FLIPFLOP	11.80mW	18.97mW	37.55mW
%Power Saved Compared With Cmos	68.56%	49.4727%	0%

Table.3 Power analysis of 3-BIT SIPO register

CIRCUIT	PFAL	ECRL	CMOS
3-BIT SIPO REGISTER	32.67mW	45.986mW	93.841mW
%Power Saved Compared With Cmos	68.56%	49.4727%	0%

From above tables it is clear that PFAL performs better than the other adiabatic techniques and conventional CMOS technique the graphs which produced below will depict us the clear technique which performs the better power saving

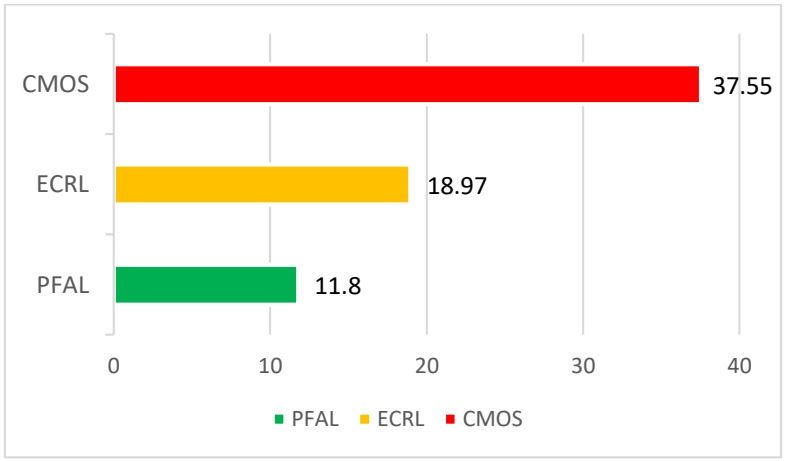

FIG.12 Graph of power consumed in D-Flipflop (mW)

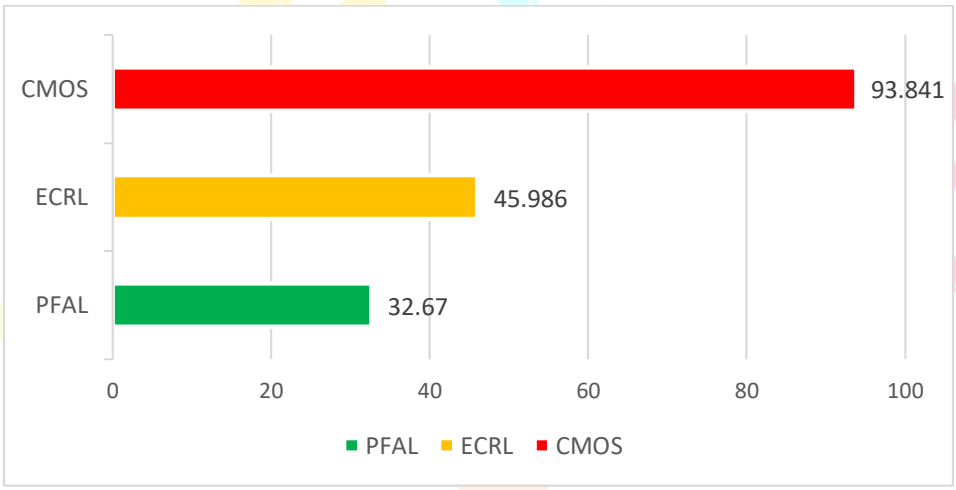

FIG.13 Graph of power consumed in 3-bit SIPO register (mW)

Table.4 Transistor count of Different circuits using low power adiabatic logic

CIRCUIT	PFAL	ECRL
D-FLIPFLOP	40	30
3-BIT SIPO REGISTER	120	90

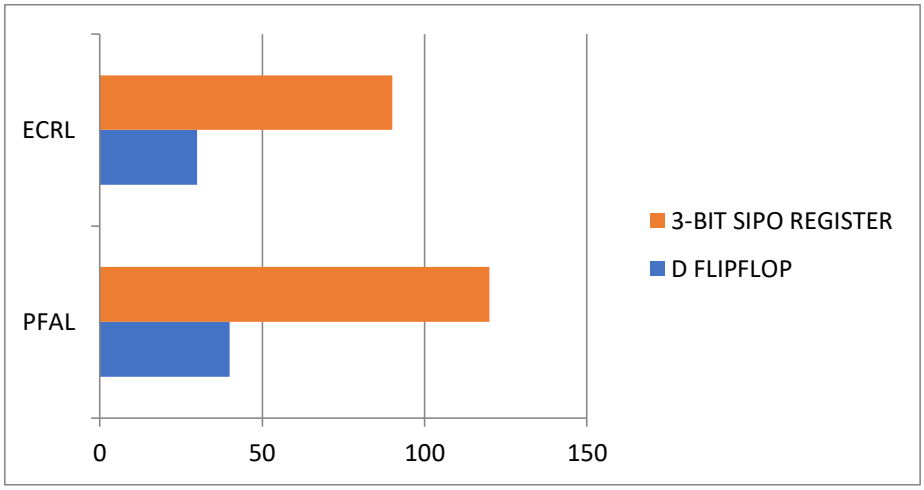

FIG.14 Graph of number of transistors used in different sequential circuits in adiabatic techniques

Table.5 Power analysis of Different circuits using low power adiabatic logic

CIRCUIT	PFAL	ECRL
D-FLIPFLOP	11.80mW	18.97mW
3-BIT SIPO REGISTER	32.67mW	45.986mW

4. CONCLUSION

In this paper we designed and implemented different sequential circuits and analysed the power consumption of different adiabatic techniques. And here we implemented sequential circuits D-flipflop and 3-Bit SIPO register and power consumption is compared between PFAL, ECRL and CMOS. After analysing the power, we found that PFAL is the power efficient. Even though ECRL also saved the power, PFAL showed us the best power saving capability.

Here we can conclude that adiabatic techniques are for sure power efficient techniques. But there are also some draw backs while using them. These techniques may become problematic for the devices in which there is a area concern and they have to compromise with the time delay also. Definitely the techniques can be implemented where area is not important and power is the most important factor. Hence, we conclude that these are mostly preferable for applications which are power concerned.

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