IJNRD.ORG ISSN : 2456-4184
INTERNATIONAL JOURNAL OF NOVEL RESEARCH AND DEVELOPMENT (IJNRD) | IJNRD.ORG
An International Open Access, Peer-reviewed, Refereed Journal

DESIGN OF LOW POWER SYNCHRONOUS COUNTER USING ADIABATIC TECHNIQUES

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***Abstract*:** In the designing of VLSI circuit's power dissipation has become a major concern. So, by reducing power dissipation we can attain our low power circuit. Excessive power consumption can negatively impact circuit reliability, resulting in higher maintenance costs, which elevates the cost of cooling system and packaging. As, with the advancement of electronic circuits which are dealing with the digital circuitry are implemented with the use of CMOS technology. The simultaneous pursuit of high performance and low power consumption remains a paramount concern in contemporary integrated circuit design. Various adiabatic techniques can be used for minimizing the power Consumption. In the quest for ever-more efficient digital integrated circuits (ICs), adiabatic logic techniques have emerged as a promising alternative to traditional CMOS logic design. Adiabatic techniques aim to reduce power dissipation during signal transitions, potentially leading to significant improvements in circuit performance and energy efficiency. To evaluate their effectiveness, these techniques have been compared against established CMOS logic design principles in the context of specific circuit implementations, such as synchronous counters. The sequential circuit (Synchronous counter) is implemented with the use of adiabatic techniques like ECRL, 2N-2N2P etc

Keywords - Complementary Metal Oxide Semiconductor(CMOS), N-channel metal-oxide semiconductor (NMOS), P-channel metal-oxide semiconductor (PMOS),Efficient Charge Recovery Logic(ECRL),Direct Current Diode Based Positive Feed Back Logic(DC DB PFAL)

I.INTRODUCTION:

In this work, we focus on applying adiabatic logic design principles to implement fundamental sequential circuits. Sequential circuits, such as flip-flops, registers, and counters, are the backbone of digital systems, enabling information storage and processing over time. Their ability to retain past states (memory) differentiates them from combinational circuits, whose outputs solely depend on the present inputs. This inherent memory allows sequential circuits to exhibit dynamic behavior, making them crucial for applications like digital counters, shift registers, and finite state machines. Here, we explore the implementation of these essential sequential circuit elements using established adiabatic techniques. This approach aims to significantly reduce power consumption compared to conventional CMOS logic design, thereby extending battery life and enhancing system efficiency. The subsequent sections will delve into the implementation details and analyze the achieved power reduction through rigorous testing

II.METHODOLOGY:

2.1FLIPFLOP:

Flip-flops are single-bit memory elements with two stable states (typically represented as O and 1). They can be triggered by clock signals to switch states. Common types include SR, D, JK, and T flip-flops. Master-slave configurations are also used. The paper specifically discusses D flip-flops, which store data based on the clock input. When the clock is high, the data input is captured at the output. When low, the output retains its previous value. These are the simplest flip flops which are used as basic building blocks for many other circuits

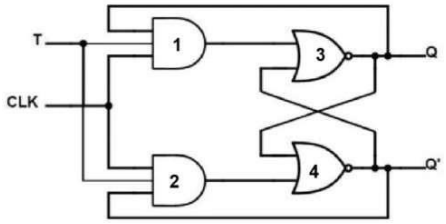


Fig.1 T flip-flop

2.2REGISTERS

A SISO register is constructed by cascading multiple D flip-flops. These flip-flops are connected in a chain-like manner, where the output of one flip-flop serves as the input to the next. A clock signal synchronizes the operation of the register. When the clock pulse arrives, the data at the input is captured by the first flip-flop, and the existing data within each flip- flop is shifted one position down the chain. The data from the last flip-flop in the chain becomes the serial output, emerging one bit at a time according to the clock signal.

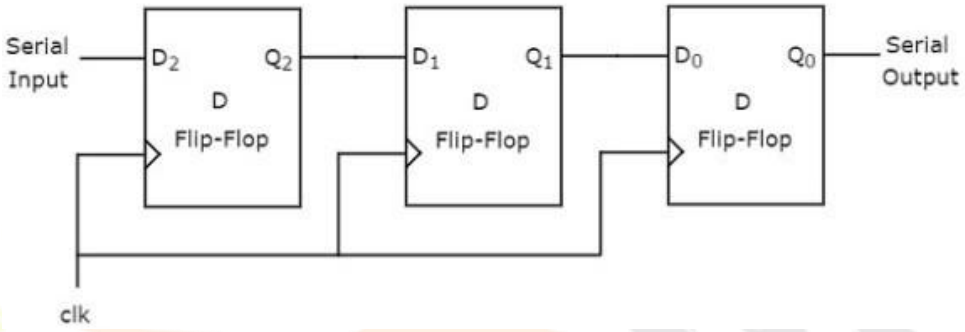


Fig.2 SISO Register

2.3 CMOS METHOD

The shape of a CMOS community to realize any arbitrary Boolean characteristic is proven in fig .Here, rather than the use of a unmarried pull-up transistor, a community of pMOS transistors is used as pull up. The pull-down circuit is a community of nMOS transistors, as it's miles achieved within side the case of an nMOS realization.CMOS logic circuits, pull-up networks (PUNs) and pull-down networks (PDNs) play a critical role in establishing a well-defined and stable voltage level at the output. These networks function in a complementary manner, ensuring a clear and unambiguous logic state ('0' or '1').

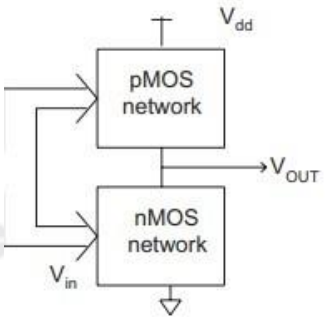


Fig.3 CMOS logic

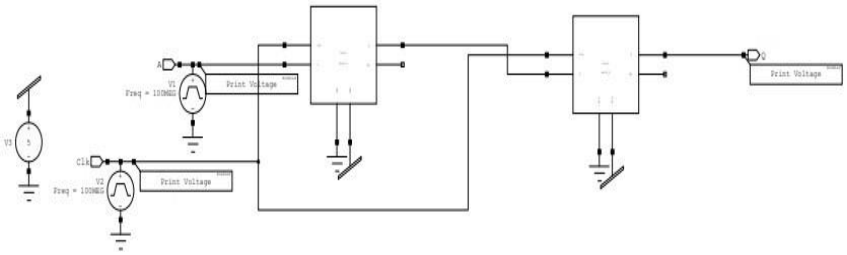


Fig.4. CMOS 2 Bit Counter

2.4 LOW POWER ADIABATIC TECHNIQUES

In the context of adiabatic logic, the term refers to a process where minimal energy exchange occurs between the circuit and its surroundings during switching operations. Here adiabatic techniques refer to the loss of power in circuit without considering the external losses i.e. environment related power loss. Adiabatic techniques use reversible logic to save power while the process of charging and discharging is going on in the circuit. It has two phases one is pre-chargeand other is charge recovery. Pre-charge phase is before delivery of energy and charge recovery phase is at recovery of the energy. Adiabatic techniques have two types they are fully adiabatic and quasi (or) partial adiabatic based on recovery of charge. When it recovers only some part of charge then it is partial (or) quasi if recovers completely then it is fully adiabatic. Fully adiabatic techniques are very complex to design and implement so here we are using quasi adiabatic techniques in this paper. Some examples of quasi adiabatic techniques are PFAL, ECRL, and 2N-2N2P etc.

2.5 PROPOSED DCDBPFAL LOGIC

DC-DB PFAL logic offers an enhanced adiabatic logic design by incorporating an NMOS diode and a DC voltage source. This configuration, positioned between the pull-down NMOS transistors and ground, provides two key benefits. First, it enables precise control over the discharge path through level shifting. Second, it reduces the dischargerate within the circuit. The level shifting further minimizes leakage current in the output transistor and reduces its gate- to-source voltage (Vgs), leading to improved overall efficiency.

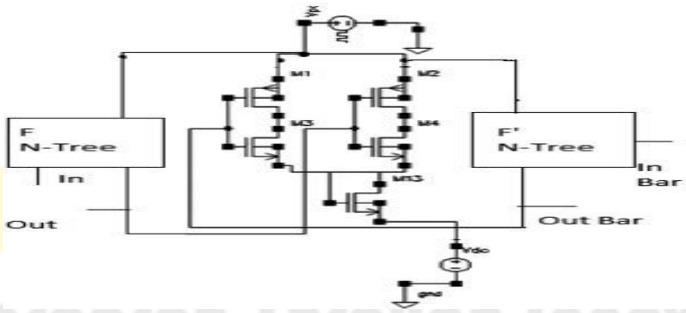


Fig.5 DCDB PFAL logic

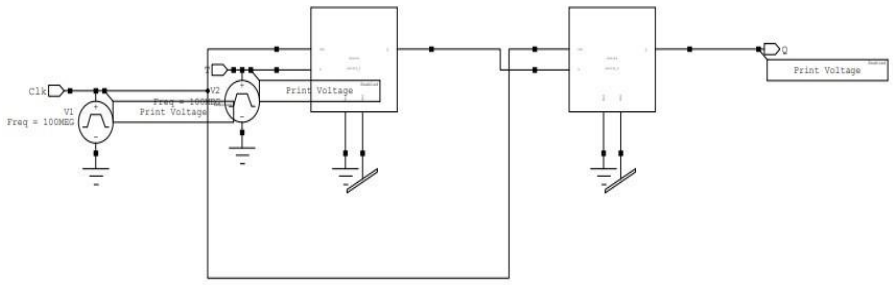


Fig.6 DCDB PFAL 2 Bit counter

2.6 PROPOSED ECRL LOGIC

ECRL stands for Efficient Charge Recovery Logic. It comprises of two cross-coupled and two PMOS devices and complementary functional blocks are connected to the PMOS. As shown in figure

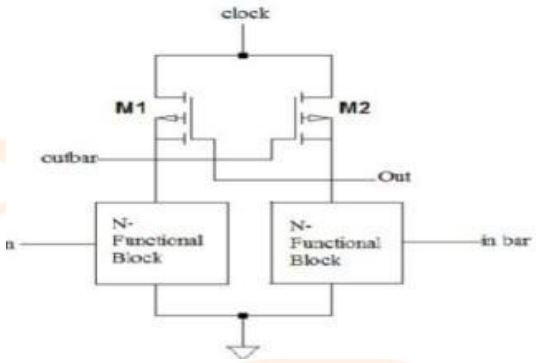


Fig.7 ECRL logic

The adiabatic logic ECRL 2 Bit Counter can be implanted as shown in figure using Tanner EDA

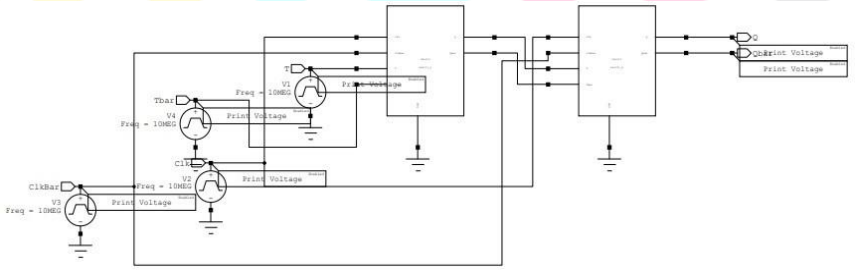


Fig.8 ECRL 2 Bit counter

2.7 PROPOSED 2N-2N2P LOGIC

The 2N-2N2P logic family builds upon the 2N-2P design, specifically addressing the issue of coupling effect. This improvement is achieved by replacing the latch with a configuration that utilizes both pMOSFETs and nMOSFETs in a cross-coupled manner. This cross-coupling of nMOSFETs ensures that the outputs remain stable (non-floating) duringa significant portion of the recovery phase.

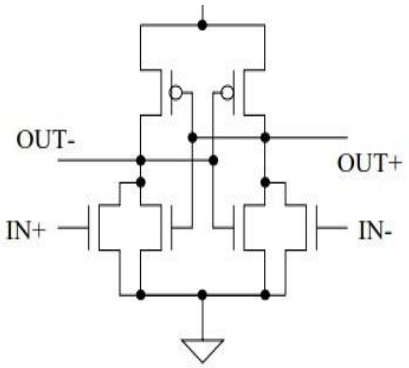


Fig .9 2N2N2P logic

The adiabatic logic 2N-2N2P 2 bit counter can be implemented as shown below in the figure using Tanner EDA.

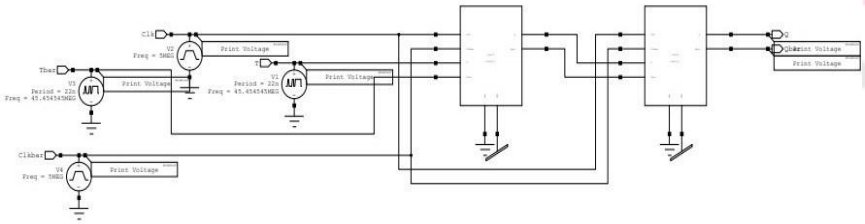


Fig.10 2N2N2P 2Bit counter

2.8 IMPLEMETATION OF SERIAL IN SERIAL OUT SHIFT REGISTER USING LOW POWER ADIABATIC TECHNIQUES

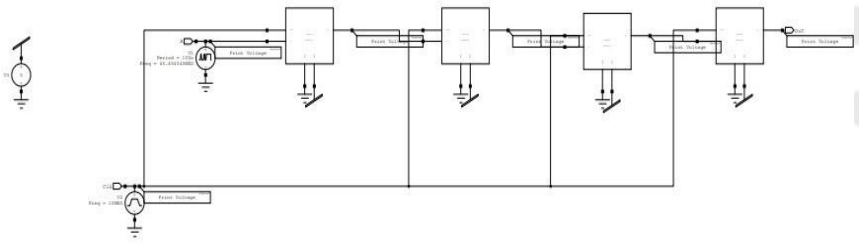


Fig.11 2 SISO Register using DCDB PFAL

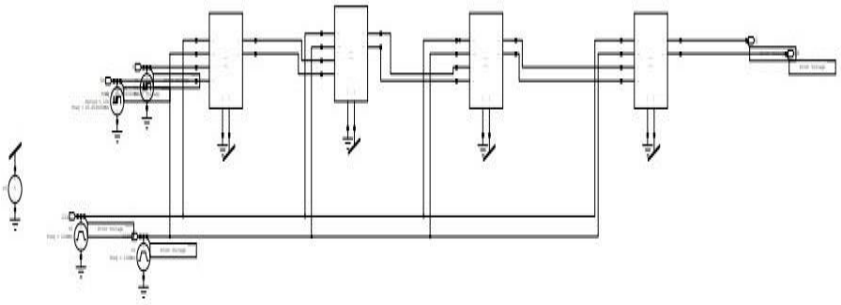


Fig.12 4 SISO Register using 2N2N2P

III.SIMULATION RESULTS AND DISCUSSIONS

Synchronous counter is implemented using ECRL, 2N2N2P AND DCDB PFAL partially adiabatic techniques. Thepower calculations are made and depicted below. The power analysis are made at different frequency ranges

Table.1power results at 10 MHz 2 bit counter

TECHNIQUE	POWER(m W)	NO.OF TRANSISTORS
CMOS	42.75609	40
ECRL	20.01354	56
2N-2N2P	19.58075	72
DC DB PFAL	11.67692	120

Table.2 power results at 100 MHz 2 bit counter

TECHNIQUE	POWER(m W)	NO.OF TRANSISTORS
CMOS	72.447	40
ECRL	46.494	56
2N-2N2P	54.613	72
DC DB PFAL	28.107	120

SISO Shift Register is implemented using 2N2N2P AND DCDB PFAL partially adiabatic techniques. The power calculations are made and depicted below. The power analysis are made at different frequency ranges.

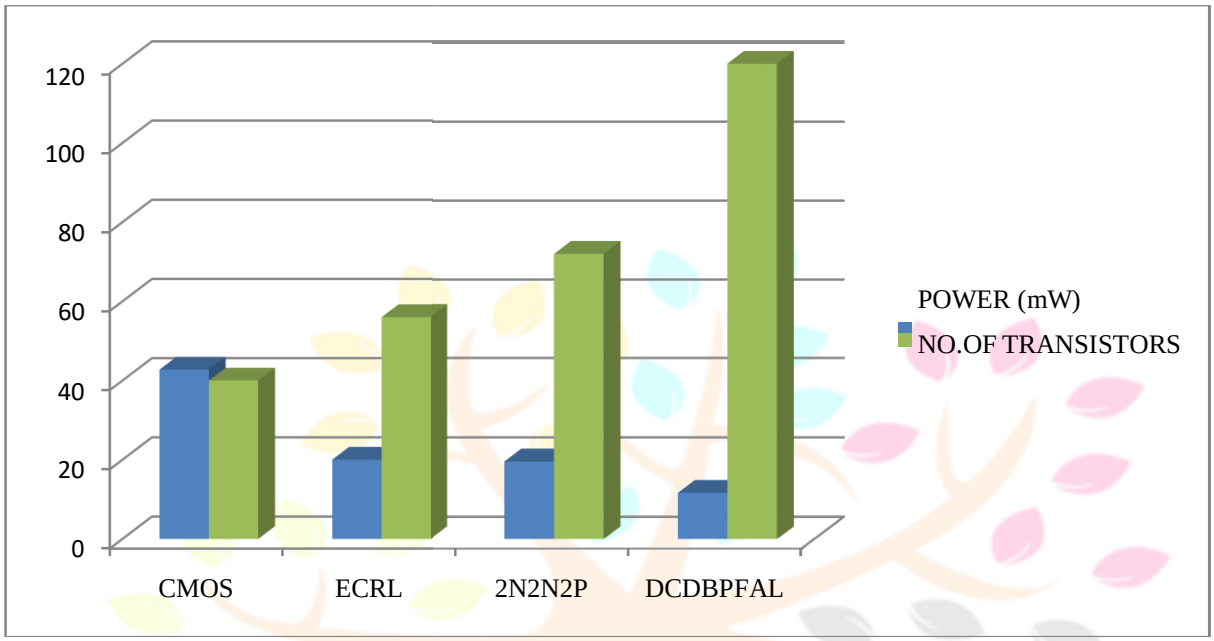
Table 3.Analysis of SISO shift register at 10 MHz frequency

TECHNIQUE	POWER(m W)	NO.OF TRANSISTORS
2N2N2P	54.13	128
DCDBPFAL	36.97	208

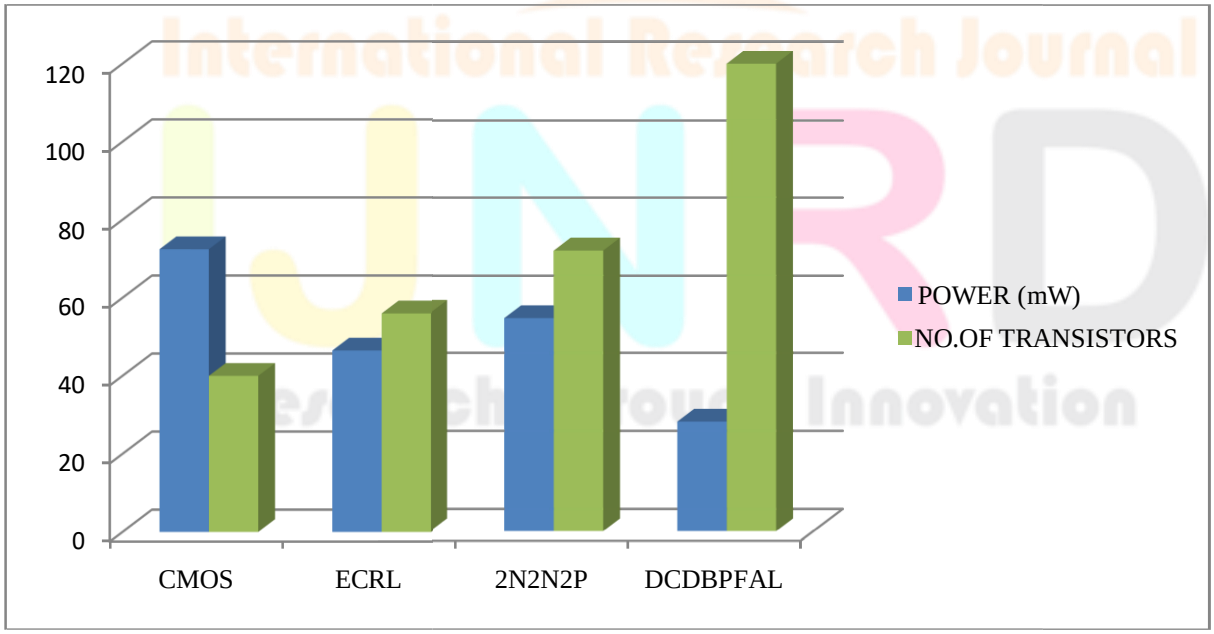
Table 4.analysis of SISO shift register at 100 MHz frequency

TECHNIQUE	POWER(m W)	NO.OF TRANSISTORS
2N2N2P	72.55	128
DCDBPFAL	55.58	208

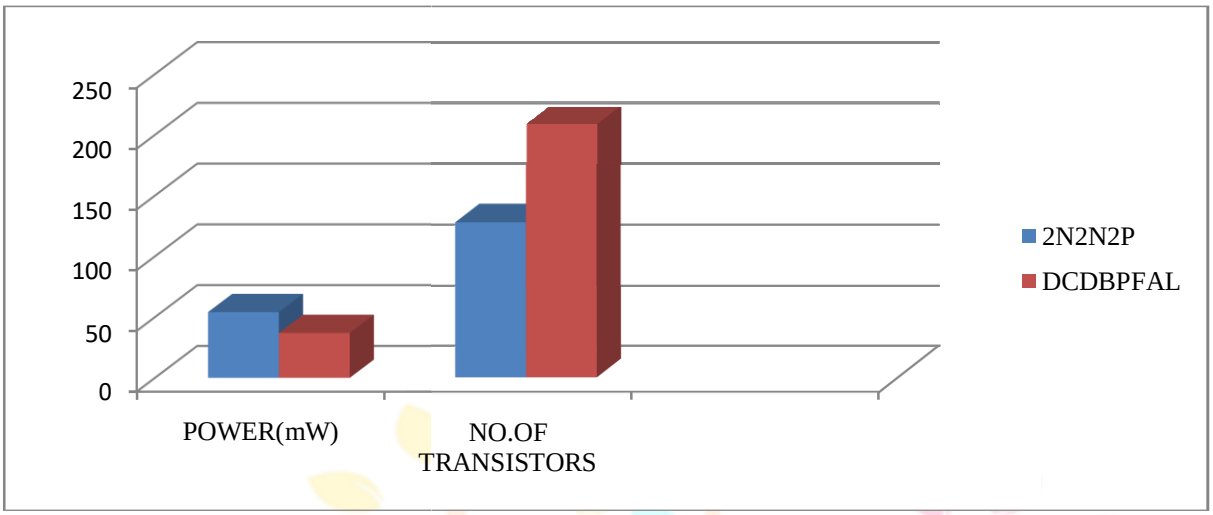
To gain a clearer understanding of how different logic design techniques fare in terms of power efficiency at varying frequencies, we'll delve into graphical representations. These graphs will showcase the power consumption of DCDB PFAL, alongside other adiabatic techniques and conventional CMOS, across a range of frequencies. By analyzing thesevisuals, we can pinpoint the technique that demonstrably achieves the best power savings under different operating conditions. This approach emphasizes the role of the graphs in revealing the most efficient technique and avoids simplystating the conclusion based on tables.



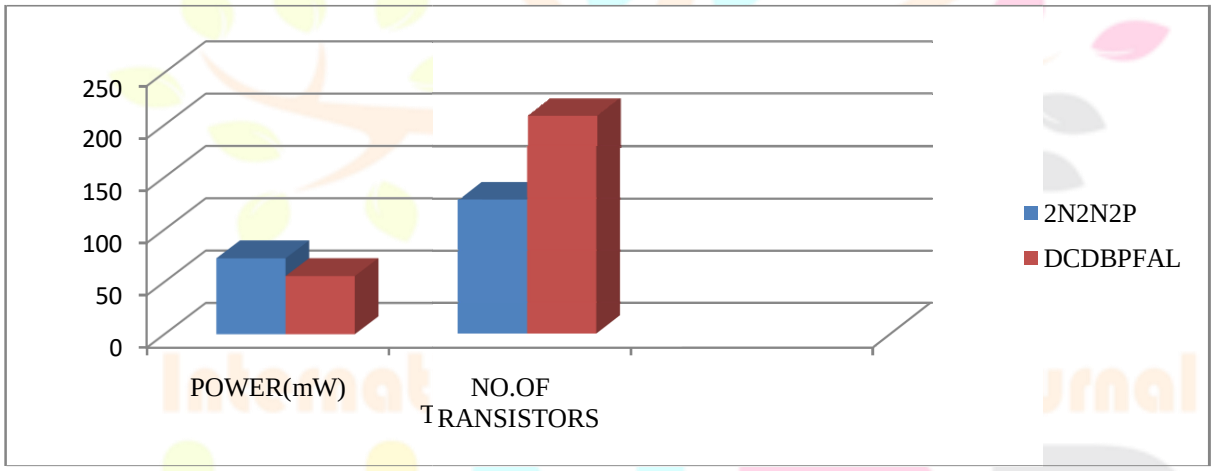
Graph.1 Power results at 10 MHz 2 Bit Counter



Graph.2 Power results at 100MHZ 2 Bit Counter



Graph.3 Power results at 10 MHz SISO shift register



Graph.4 Power results at 100 MHz SISO shift registers

IV CONCLUSION

We first implemented a synchronous counter circuit using ECRL, 2N2N2P, and DCDB PFAL partially adiabatic techniques. Based on a power analysis of the synchronous counter in different partially adiabatic techniques, the DCDB PFAL technique demonstrated the lowest power consumption among ECRL and 2N2N2P. Therefore, we implemented a Serial in Serial out (SISO) shift register and D flip-flop using the DCDB PFAL adiabatic technique. All these circuits are implemented in TANNER EDA software

In conclusion, adiabatic techniques demonstrably offer significant power efficiency benefits. However, their Implementation may incur area overhead and introduce potential delays. Therefore, these techniques are most Advantageous for applications where power consumption is the primary concern and chip area is not a critical constraint. Examples include battery-powered portable devices and energy-harvesting systems.

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