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COMPARISON AND PERFORMANCE ANALYSIS OF RING OSCILLATOR AND CURRENT STARVED VCO IN 45-nm CMOS TECHNOLOGY

[1]*L. Vasu,*[2]*V. Baby Harini Sree,* [3]*T. Deepa,*[4]*D. V. Suresh,* [5]*K. Tharun Kumar, & K. Lakshmi Narayana*

[1]*Assistant Professor, Dept of ECE, PBR VITS, Kavali, Andhra Pradesh, India.*

[2-6]*UG Students, Dept of ECE, PBR VITS, Kavali, Andhra Pradesh, India.*

Abstract- **This Project presents a comprehensive comparison and performance analysis of ring oscillators (ROs) and current-starved voltage-controlled oscillators (VCOs) implemented using 45-nm CMOS technology. Both ROs and current-starved VCOs are fundamental building blocks in modern integrated circuits, particularly in frequency synthesis and clock generation applications. Understanding their performance characteristics and trade-offs is crucial for optimizing VLSI circuit designs.**

This Project begins with a detailed overview of ROs and current-starved VCOs, highlighting their operating principles and design considerations in 45-nm CMOS technology. Key performance metrics, including oscillation frequency, power consumption, are identified for comparison. Simulation experiments are conducted using Tanner Tool and transistor models toevaluate the performance of ROs and current-starved VCOs under various operating conditions. The results of the comparative analysis are presented and analyzed, revealing the strengths and weaknesses of each oscillator architecture.

I.INTRODUCTION

The design of clock circuit for microprocessor to carrier synthesis in wireless communication needed different Oscillator circuits. The PLL used in wireless devices, PLL needed Oscillator. Oscillator are integral part of many electronic systems application rang from clock generation in microprocessor to carrier synthesis in cellular telephones requiring vastly different oscillator topologies and performance parameter. Recently the explosive growth in wireless communication and the advances in complementary metal oxide semiconductor (CMOS) technology made it possible to implement high frequency oscillator with CMOS technology. There are different oscillators such as waveform oscillator and resonant oscillator. The wave form oscillator include Ring oscillator and relaxation

oscillator, similarly resonant oscillator having LC oscillator and Crystal oscillator. LC oscillator has low phase noise but low frequency swing. They are used in wireless application. On the other hand the ring oscillator is widely used in integrated circuit. Ring oscillators are being used by semiconductor foundries to monitor power dissipation, delay, and jitter of fabricated CMOS inverters. On the basis of result of measured frequency pattern we accept or reject the IC. Ring oscillator also occupies less chip area as they do not have inductor as compared to LC tank oscillator. As the LC oscillators are less prone to noise.

II.EXSTING SYSTEM :

In high-speed data communication systems, clock recovery is one of the most critical factors determining the overall bit error rate of the system. One technique for high performance clock recovery is to use multi phase clock signals sampling incoming data. In this approach, accuracy of the tap-to-tap spacing determines the phase noise of clock recovery. In addition, for micro programmed very large scale integration (VLSI) systems, the multi phase clock signals are commonly used to generate various control signals for data paths.

Therefore, as clock speeds increase, much more finely spaced multi phase clock is needed. Conventional CMOS ring oscillator have been popularly used for these applications, because they can provide multi phase clock signals due to their high-speed operation and simple structure. In the conventional ring oscillators, the oscillation frequency is determined by the inverse of twice the sum of the individual delays. Furthermore, the minimum tap-to-tap spacing in the conventional ring oscillator cannot be smaller than two inverter delays. Here, we have to add more inverters to obtain more output phases, which in turn decreases the maximum operating frequency. To obtain a smaller spacing, an array oscillator comprised of a series of coupled ring oscillators that can achieve a delay resolution down to a inverter delay divided by the number of rings were proposed . Because this circuit is based on an array structure, however, the number of the multi phase outputs is limited to the multiples of the number of stages in the ring.

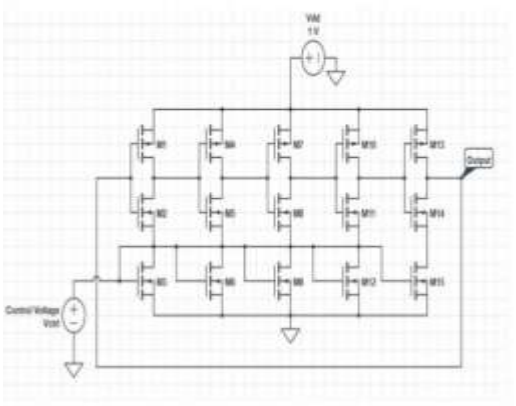


Fig : Circuit diagram of Ring VCO

The switching frequency at each gate is inversely proportional to both the number of gates in the ring and the gate delay of each individual gate.

A voltage-controlled oscillator is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency. Consequently, a VCO can be used for frequency modulation (FM) or phase modulation (PM) by applying a modulating signal to the control input.

A VCO is also an integral part of a phase-locked loop. VCOs are used in synthesizers to generate a waveform whose pitch can be adjusted by a voltage determined by a musical keyboard or other input.

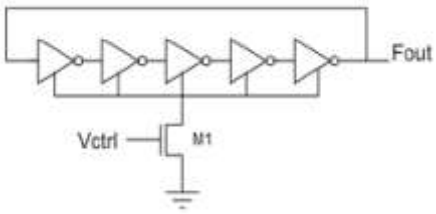
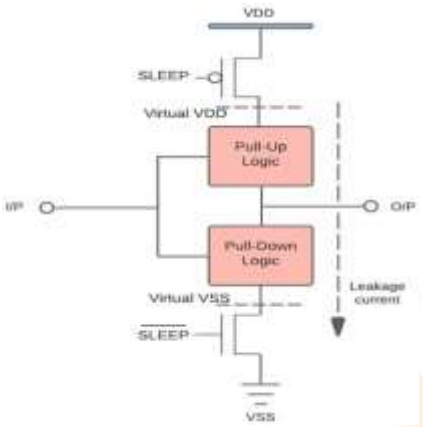


Fig: Circuit Diagram of Voltage Control Oscillator

III.PROPOSED SYSTEM

In the proposed method 2 VCO circuits are designed namely , current starved VCO, Power gated CSVCO. Cascading the inverter blocks with a feedback gives a 'Ring' configuration to the oscillator. Furthermore, biasing circuit is included in the design to introduce the control voltage into the oscillator for

control over frequency of oscillations. Hence, it's called Ring VCO . Another VCO under discussion is an improved version of Ring VCO, called Current Starved VCO. The operation is similar to Ring VCO with additional MOSFETs are added so as to operate as current sources with the MOSFETs that operate as



inverter.

This technique is known as current starving. The current source produces control current to lower the threshold voltage of inverter transistors, which increases the effective drive resistance and thus increases the delay. With lesser power dissipation, decreased phase noise, improved waveform generation and many more, the design out does the Ring VCO in nearly all fields, except area since the transistor count is nearly double. Hence, area should be traded off with other parameters for better oscillations for Current Starved VCO deployment.

Even with reduced dependence on power supply noise, particular applications demand higher oscillation frequency while functioning. Hence, to decrease this delay the concept of Power gated CSVCO is considered. The connections are altered by providing Power gated CSVCO inverter input signal to PMOS earlier than to the NMOS and output changing becomes faster.

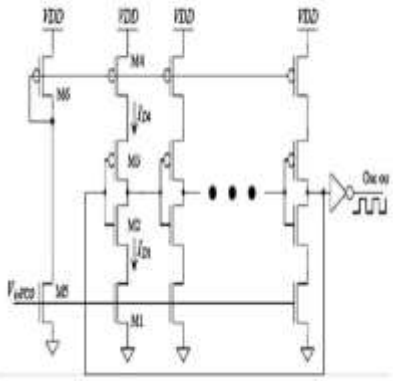


Fig: n-Stage current starved VCO

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing.

Fig:Circuit diagram of Power Gating Technique

ADVANTAGES

- Low Power Consumption
- Frequency Tunability
- Low Phase Noise
- Frequency Stability
- Power Consumption

IV.RESULTS AND DISCUSSIONS

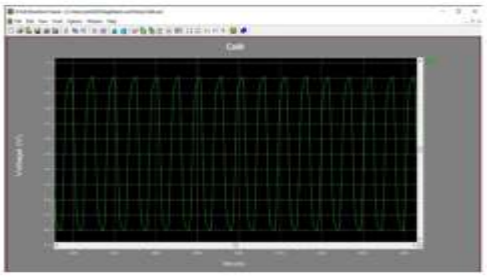


Fig: Simulation Results of Ring Oscillator

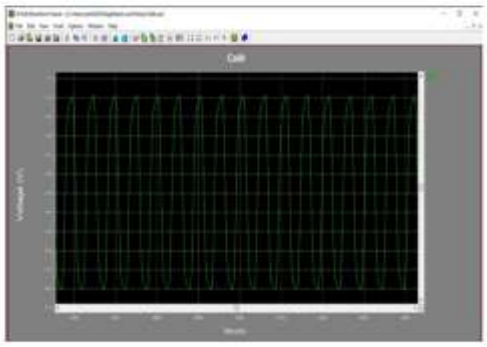


Fig: Simulation result of Ring VCO

Fig: Simulation result of CSVCO

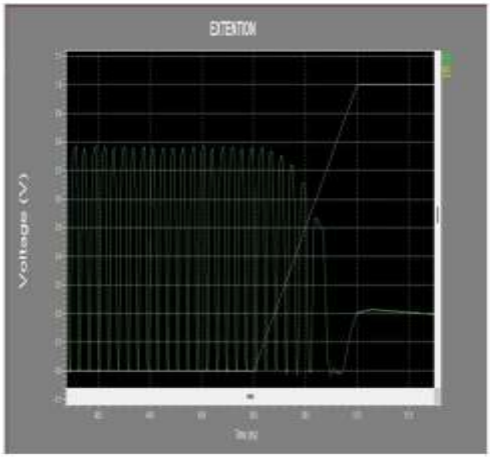


Fig: Simulation result of Power gated CSVCO

V. CONCLUSION AND FUTURESCOPE

The proposed power gated 5-stage CSVCO have been successfully designed and simulated using Tanner EDA tool with 45nm technology. From the simulation it can be observed that the proposed power gated ring vco generates oscillations only in active mode and the power is saved in the sleep mode.

FUTURE SCOPE:

Since chip sized is fixed, and It is essential to add more logic into the chip for inserting additional features, in our extension we will design an area efficient vco.

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