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Optimised design of low power D-flip flop : A Comprehensive Review

Harsha Vardhan N[1],
KB Ramesh[2]

[1]2nd year , Electronics and Instrumentation Engineering
RV College of Engineering, Bengaluru.
harshavardhann.ei22@rvce.edu.in
[2] Associate professor, Department of Electronics and instrumentation Engineering,Bengaluru
RV College of Engineering, Bengaluru.
rameshkb@rvce.edu.in

Abstract :
This research paper conducts a comprehensive review of pioneering studies centred around the design and optimization of Carbon Nanotube Field-Effect Transistor (CNTFET)-based D flip-flops for advanced nanoscale electronic circuits. One study focuses on exploring various parameters of CNTFETs derived from prior research and meticulously analyses the impact of manipulating parameters, such as decreasing the diameter and number of CNTs, on the leakage current and power consumption of a proposed D flip-flop. The outcomes showcase a substantial reduction in both leakage current and power consumption, with an average of only 10.306 nW leakage power—an exceptionally low value compared to contemporary circuits. This study emphasises the significance of tailored CNTFET characteristics, including a 5 nm oxide thickness and 16 nm CNT length, to achieve optimal D flip-flop performance while minimising overall power consumption.Another study introduces a novel D flip-flop design using CNTFETs, operating on a True Single Phase Clock (TSPC) and employing a master-slave TSPC latch in a cascaded configuration. Through extensive simulations, the proposed flip-flop exhibits superior performance metrics, including reduced setup time, hold time, clock to output propagation delay, low clock load, and overall low power consumption. Comparative analysis against existing flip-flops, such as NAND-based logic, Transmission gate logic-based MUX, C^2MOS, and TSPC flip-flops, reveal significant advantages in terms of both power and energy efficiency. The proposed flip-flop emerges as a promising candidate for integration into low power and energy-efficient Very Large Scale Integration (VLSI) systems.

This review consolidates insights from these studies, highlighting the synergies and advancements achieved in CNTFET-based D flip-flop designs.The review also analyses on the combination of different techniques used in the studies referred. The collective findings contribute to the ongoing exploration of nanoscale devices for high-performance and low-power circuit applications, showcasing the potential for transformative advancements in VLSI systems.

I. Introduction :

In recent years, the field of nanoscale electronics has witnessed a paradigm shift, with a growing emphasis on exploring novel semiconductor devices to replace traditional Complementary Metal Oxide Semiconductor (CMOS) technology. This transition is driven by the pursuit of superior device physics, increased efficiency, and reduced power consumption in future nanoscale electronic circuits. Carbon Nanotube Field Effect Transistors (CNTFETs) and Nanowire transistors have emerged as promising alternatives due to their potential to revolutionise the landscape of electronic devices, including processors, GPUs, and RAMs. As these devices continue to shrink in size, their capacity has increased while simultaneously enhancing energy efficacy and operational speed, presenting a significant leap forward from silicon transistors.

CNTFET-based circuits, predicted to be three times faster than silicon transistors while operating at comparable power levels, offer a compelling avenue for achieving enhanced performance in electronic circuits. This surge in interest is underscored by the identical operating characteristics of CNTFETs and silicon-based MOSFETs, where electrons move from source to drain. Notably, CNTFET technology gains prominence due to its high channel mobility and improved gate capacitance versus voltage features, addressing challenges associated with the reduction of oxide thickness[1] in double-gate MOSFETs.

Researchers are actively exploring the potential of CNTFETs in digital circuit design, with a particular focus on realising the benefits in the realm of sequential circuits such as D flip-flops. The transition to nanoscale technologies is driven by the relentless pursuit of overcoming limitations inherent in silicon MOSFETs, such as short channel effects, to achieve low power consumption, reduced area, and high performance in essential memory storage units like D flip-flops.

This review consolidates insights from two seminal papers that contribute significantly to the advancements in CNTFET-based D flip-flop design.One paper delves into the manipulation of CNTFET parameters to optimise leakage current and power consumption, while the other paper introduces a novel D flip-flop design based on True Single Phase Clock (TSPC) operation. Both papers demonstrate the potential of CNTFET technology in achieving low power consumption and high energy efficiency, making them pivotal in the ongoing discourse on the future of VLSI systems.

The remainder of the paper is organised as follows: Section II states the theoretical background, Section III presents the related works, Section IV outlines the methodology, section V provides flip flop optimization, section VI provides the experimental outcomes, section VII illustrates the simulation result, section VIII exhibits analysis

of the current and prospective schemes in comparison and finally, Section IX provides conclusion.

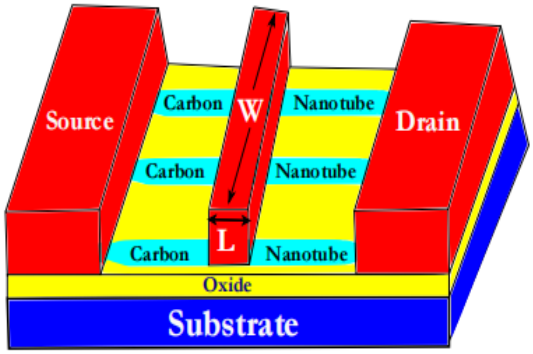

Fig. 1: Schematic of Carbon Nanotube Filed Effect Transistor (CNTFET)

II. Theoretical Background :

A. Carbon Nanotube Field Effect Transistor (CNTFET)

A field effect transistor using carbon nanotubes refers to a field effect transistor that uses a single CNT or CNT array as a channel material instead of bulk silicon in the conventional MOSFET structure. The core material of CNTFET is carbon nanotube, which are carbon allotropes with a tubular nanostructure.[1]

CNTFET are the transistors that utilise Carbon Nanotube (CNT) as a carrier channel. Carbon nanotubes are rolled up in the form of graphene sheets along a chiral vector. Heavily doped CNT regions inCNTFET are considered to be drain/source regions whereas CNT that acts as the channel region is undoped. The schematic of the Carbon Nanotube Field Effect Transistor is shown in Figure-1.[2]

B. D Flip-flop

D flip-flops are a significant part of today's digital electronics . It is a basic memory cell giving an output equal to its data input, provided a clock signal is supplied. If the clock is not enabled, then the output stores its previous value. The attributes of this flip-flop can be explained through the following Table I.[2]

TABLE I. CHARACTERISTICS TABLE OF D FLIP-FLOP

Previous Output, Q_n	Input, D	Current Output, Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

C.Leakage Current

The cause of static power consumption is leakage current, which is a mix of subthreshold and gate-related currents.

$$I_{leak} = I_{sub} + I_{ox} \qquad (1)$$

where, I_{leak}, I_{sub} and I_{ox} denote oxide leakage current,subthreshold leakage current and gate-oxide leakage current respectively. [1]

a. Subthreshold leakage current :

Sufficient supply voltage and threshold voltage are required for subthreshold leakage current, according to an equation presented by [1]A. Chandrakasan, W. J. Bowhill and F. Fox [6]:

$$I_{sub} = K_1 W e^{-V_{th}/nv_o} \qquad (2)$$

where, K1 and n are derived experimentally, W and Vth are gate width and the threshold voltage respectively, while Vo in the exponents being the thermal voltage. Now, Vo is around 25 mV at room temperature, which rises linearly with temperature. Again,Vo will begin to climb if Isub increases to the point that heat begins to accumulate, which could result in thermal runaway.[1]

Equation (2) offers two approaches to reduce I_{sub}. Initially,[1] we can deactivate the power supply, effectively setting it to zero, leading to a capacitor with zero influence. Alternatively, we can elevate the threshold voltage, Vth, whose negative exponent can exert a substantial effect even with minor adjustments. However, adjusting Vth comes at the expense of reduced speed. The first method introduces a concern related to state loss, while the second is associated with a potential loss in performance.
The gate width, W of a transistor plays a vital role in subthreshold leakage current , but for calculation purpose and ease of estimation designers consider the total width of all transistors in the processor as an effective solution to calculate total subthreshold leakage current.

b. Gate-oxide power leakage :

Leaks in gate oxide are less studied than subthreshold leaks. For our purposes, it is sufficient to simplify the Chandrakasan, Bowhill, and Fox[6] equations to account for the key factors.

$$I_{ox} = K_2 W \left(\frac{V}{T_{ox}}\right)^2 e^{-\alpha T_{ox}/v} \qquad (3)$$

where, K2 and □ are calculated experimentally. The oxide thickness, T_{ox}, is the term of interest.Raising the oxide thickness (T_{ox}) undoubtedly reduces gate leakage. However, this poses a challenge since T_{ox} needs to decrease to counteract the short channel effect, impacting the transistor's efficiency. Consequently, increasing T_{ox} is not a viable solution. Researchers are persistently exploring advanced dielectric gate insulators of high quality. Similar to subthreshold leakage, the collective mesh width of the mould serves as a practical approximation of the overall oxide leakage.

c. Low-Power Architectural design :

The leakage contribution of pipeline implementation is similar to the basic serial case, inclusive of additional gates with the latch, as both subthreshold and oxide leaks are contingent on the total gate width or the quantity of gates. Implementing pipelines allows for operation at lower voltages, leading to decreased dynamic and static power usage compared to serial systems. Although low-voltage parallel deployment is possible, it requires nearly double the hardware. Depending on experimental parameters, parallel configurations may consume more power than serial configurations, offsetting dynamic power savings. Consequently, pipeline processing is more energy-efficient, with half the hardware of parallel systems, resulting in reduced power loss and operation at a lower voltage. Overall, pipeline processing demonstrates diminished dynamic and static power consumption when compared to serial processing.

D.CNTFET basics:

Carbon Nanotube Field Effect Transistors (CNTFETs) utilise Carbon Nanotubes (CNT) as carrier channels, featuring optimised parameters for reduced delay and low power dissipation. With a quasi 1-D structure, CNTFETs overcome short channel effects and provide better electrostatic control. They outperform silicon-based MOSFETs (si-MOSFET) in terms of ON current (Ion) and OFF current (Ioff), offering higher transconductance and temperature

resilience. Variations in chirality impact device characteristics, and CNTFETs are particularly suitable for Low Power Very Large Scale Integration (VLSI) applications.

III. Related works:

In this review paper we analyse the several parameters of CNTFET based D flip-flop that have been improved such as leakage power and current by different researchers mentioned in both the papers.

In 2021, T. Sharma and L. Kumre demonstrated the creation of advanced synchronous and asynchronous counter designs based on ternary logic, utilising DS type D flip-flops within Carbon Nanotube (CNT) technology [3]. The proposed methodology involves the initial utilisation of power-optimised voltage
divider networks to construct both dual shift and single shift operating circuits. Subsequently, employing a master-slave arrangement, these shifting circuits were integrated to form structures of D flip-flops. The power consumption of the described ternary D flip-flop was measured at 0.1092 µW.
In 2019, A. Karimi et al. devised a D flip-flop using Carbon Nanotube Field Effect Transistor (CNTFET) technology [4]. This circuit minimally utilises transistors, and its output is generally contingent on the CNTFET diameter and the quantity of transistors employed. Reduced transistor count results in decreased power consumption, with the average leakage power recorded at 39.906 µW.
In 2014, J. Lin implemented a circuit featuring three inverters and a feedback path [5]. This circuit operates on a conditional discharge scheme within its internal node and incorporates a static latch structure. The average leakage power for this design is 28.119 µW.
In 2005, S. H. Rasouli et al. introduced a circuit termed 'a modified hybrid latch flip-flop. This design stands out for its ability to circumvent unnecessary transitions, particularly exhibiting no delay in high-to-high transitions. The average leakage power observed in this circuit is 44.834 nW.In 2001, J. Tschanz et al. proposed a circuit known as the 'simple explicit pulse-triggered flip-flop circuit. This circuit, despite delivering high power consumption, presents a notable disadvantage. The average leakage power measured for this circuit is 3.13 µW.

IV. Methodology :

The review paper systematically analyses and synthesises contemporary research on D flip-flop designs, with a specific emphasis on minimising leakage power consumption.One method is to use energy efficient D Flip-flop by cascading the positive and negative TSPC latches using the Stanford CNTFET model and another method is to develop a circuit consists of two pVSCNT and three nVSCNT as shown in the figure 2.Through a literature review, the paper identifies key works and reconstructs circuits to replicate and validate simulation results. Theoretical frameworks from diverse sources are synthesised to develop a profound understanding of the cognitive domain in D flip-flop research. The comparative evaluation of methodologies in existing literature reveals common trends, challenges, and innovative solutions for reducing leakage power. The synthesis of knowledge culminates in a conceptual framework and guidelines for designing D flip-flops with superior power efficiency. The paper contributes to the field by highlighting consensus areas, addressing gaps, and proposing future research directions, providing a valuable resource for researchers and practitioners in the domain of low-power VLSI design.

V. Flip-flop optimization:

The flip-flop design in the first Paper [1] focuses on optimising the transistor count, power supply, and oxide thickness to achieve a standard efficiency level. The proposed scheme incorporates a single phase clock circuit along with pipeline implementation, and after careful consideration of these factors, the system is virtually proposed and implemented with satisfactory results.

In the second paper [2], an energy-efficient D flip-flop design is introduced by cascading positive and negative True Single Phase Clock (TSPC) latches using the Stanford Carbon Nanotube Field-Effect Transistor (CNTFET) model[7],[8]. Simulations are conducted in HSPICE, comparing the proposed flip-flop with existing designs. The results demonstrate that the proposed flip-flop has low power consumption, a reduced number of transistors, low clock load, low setup time, low hold time, and low clock-to-output propagation delay compared to other flip-flops. Notably, it outperforms the NAND logic flip-flop, Transmission gate logic-based MUX flip-flop, C2MOS flip-flop, and TSPC flip-flop in terms of power and energy efficiency.

To synthesise an overall flip-flop design for lower power consumption and faster operation, we can combine the insights from the papers. The design should incorporate a minimised number of transistors, optimise the power supply, consider an optimum oxide thickness, and implement pipeline techniques. Additionally, the cascading of positive and negative TSPC latches, as proposed in Paper [2], can be integrated to leverage the energy-efficient characteristics of this configuration. The combined design can
be evaluated for its performance in terms of power consumption, setup time, hold time, and clock-to-output propagation delay to ensure a comprehensive and efficient flip-flop solution.

VI. Experimental Results:

Fig. 2 depicts the envisioned D flip-flop configuration, employing two pVSCNTs and three nVSCNTs, thereby employing a reduced number of transistors. The primary focus of this configuration is the improvement of power consumption, specifically targeting the reduction of leakage power. The transistors share a uniform length of 16 nm, while the oxide thickness (T_{ox}) is maintained at 5 nm. For T1, T2, and T3 transistors, the width is 140 nm, with diameters of 0.86 nm. T4 and T5 transistors feature widths of 160 nm, with diameters of 0.86 nm and 0.98 nm, respectively. The operational states, be it open or short circuit, hinge on the condition of T2. During a high Clk, T2 operates as a short circuit, whereas during a low Clk, T2 functions as an open circuit. The control of the D flip-flop's holding voltage can be regulated by manipulating the diameter of T4. The input data is fed into T1 and T3 gates, with the initial section functioning as an inverter, yielding a value in the X node. When both data and Clk are '1,' T1 is off, and T2 and T3 are on. In this state, the current cannot traverse through the X and Y nodes, resulting in a '0' value in the X node. Consequently, T4 is activated, T5 is deactivated, and the current flows through T4, reaching the Q point, while T5 serves as an open circuit, ultimately yielding an output value of Vdd. Conversely, for data '1' and Clk '0,' T1 and T2 are off, while T3 is on, leading to '0' values in X and Y. This results in a '1' output, signifying that the value is stored when the circuit is in a low state. When data '0' and Clk '1,' T1 and T2 are both on, while T3 is off, with T3 operating as an open circuit. Current then flows through the X and Y nodes, leading to T4 turning off and T5 turning on, given the high states of nodes X and Y. Consequently, an output of '0' is obtained as T4 becomes inactive. Finally, when both data and Clk are '0,' T1 is on, and T2 and T3 are off, resulting in high and low states for X and Y nodes, respectively. T4 turns off due to the high X node, and T5 turns off due to the low Y node. As a result, the current cannot traverse through T4 and T5, culminating in an output of '0'.

The experimental outcome shows that, If both data and clock signals are in a low state, the output is low. When the data is low and the clock is high, the output is also low. In the case of high data and low clock, the output retains its previous state, remaining low. When both data
and clock signals are high, the output becomes high. The entire situation is outlined in Table II below.

Input Data, D	Clock	Output, Q_{n+1}
0	0	0 (Q_n)
0	1	0 (D)
1	0	0 (Q_n)
1	1	1 (D)

TABLE II. Truth table of the proposed circuit[1]

Data	Clock	Leakage Current (nA)	Leakage Power (nW)
0	0	3.231	3.231
0	1	2.061	2.061
1	0	1.45	1.45
1	1	34.48	34.48

TABLE III. Leakage Current and Leakage Power scenario of the proposed circuit[1]

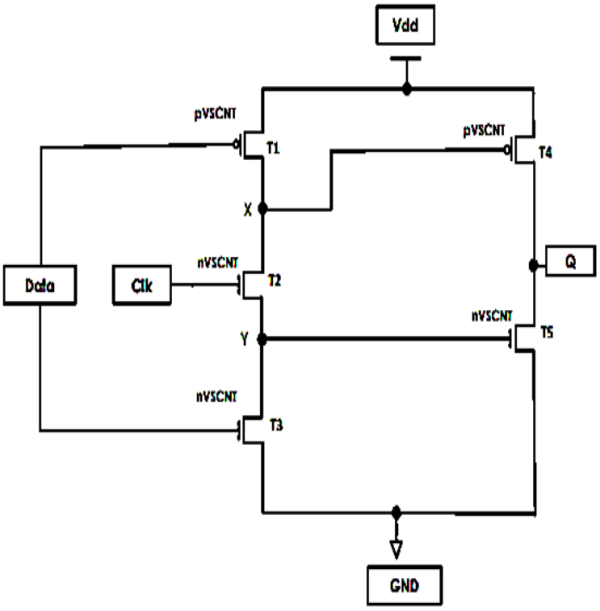

Figure 2. of D-flip flop constructed using CNTFET from 1st paper[1].

In the study of the second paper[2], we introduce a novel energy-efficient D flip-flop design achieved by cascading positive and negative True Single-Phase Clock (TSPC) latches as shown in fig.3, employing the Stanford Carbon Nanotube Field-Effect Transistor (CNTFET) model[7],[8].Table IV results show that our D flip-flop surpasses existing alternatives with lower power consumption, reduced area, decreased clock load, shorter setup time, diminished hold time, and a lower clock-to-output propagation delay. Notably, the proposed flip-flop is 99.98% more energy-efficient than the NAND logic flip-flop, demonstrating significant advantages over other designs.

In conclusion, the research introduces an innovative D flip-flop design with cascaded TSPC latches, utilising CNTFET technology for enhanced energy efficiency. Simulation results and comparative analyses against various existing flip-flops underscore the superior performance of our proposed design across multiple metrics, positioning it as a promising solution for energy-efficient digital circuits.

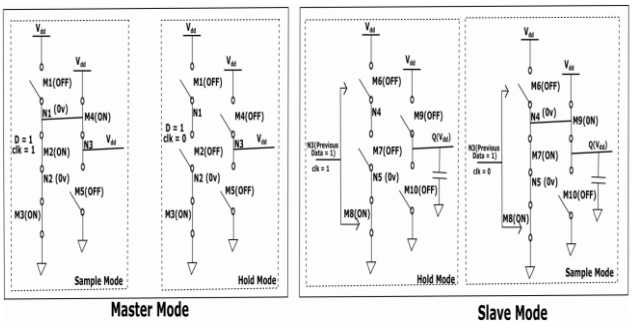

Fig. 3: Analytical operation modes of proposed Flip Flop when D is 1 and clock transition from 0 to 1 and 1 to 0 Master and Slave modes[2]

VII. Simulation Results :

The simulations conducted on the Cadence Virtuoso Platform[1] using 90 nm CMOS technology demonstrate the functionality of the proposed D flip-flop configuration. In Fig. 4, the timing diagrams reveal that when both data and clock are low, the output is low; when data is low and clock is high, the output becomes low; when data is high and clock is low, the output retains the previous state and remains low; and when both data and clock are high, the output becomes high. Table II supports the correct operation of the D flip-flop. Notably, the proposed circuit exhibits exceptional performance in terms of

leakage current and power, as indicated in Table III, with an average of 10.306 nW[1] and equal numerical values for leakage current and power due to a constant 1V supply voltage across all cases. Additionally, Fig. 5 illustrates the leakage current, from which the system's leakage power is easily calculated.

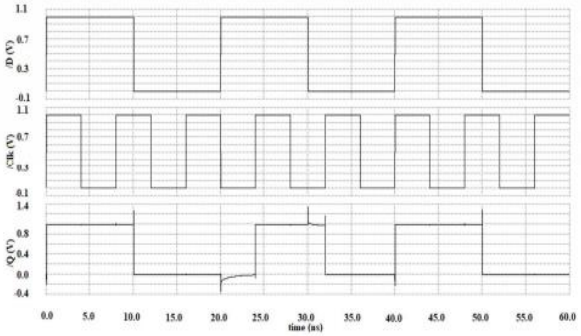

Figure 4.Output waveform of the circuit constructed using CNTFET[1].

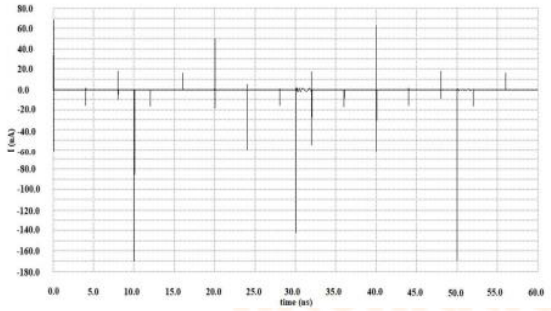

Figure 5. Leakage current waveform of designed circuit.

The simulations, conducted in HSPICE with a VDD of 2.5 V, are compared with existing flip-flops, as outlined in Table IV[2]. Energy efficiency is determined by multiplying power dissipation with the time interval of the transient analysis of the design. The timing diagram of the proposed flip-flop is depicted in

Figure 6. Results from Table IV demonstrate that our proposed D flip-flop exhibits lower power consumption, reduced area (number of transistors), decreased clock load, shorter setup time, diminished hold time, and a lower clock-to-output propagation delay when compared with existing flip-flops. Notably, the proposed flip-flop is 99.98% more energy-efficient than the NAND logic flip-flop, with significant advantages over other designs.

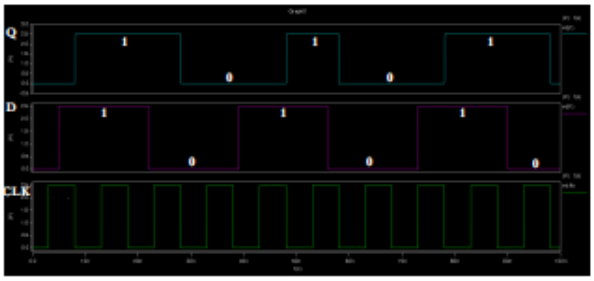

Figure 6. Timing diagram of negative edge triggered proposed D flip-flop

VIII. Comparative analysis :

The comparative analysis reveals the superior performance of our proposed flip-flop. Specifically, when contrasted with a Transmission Gate logic-based MUX flip-flop, our design consumes 99.89% less power and energy, showing lower values for setup time, hold time, and clock-to-output delay. Although the C^2MOS flip-flop exhibits only 36.8% higher power consumption than our proposed flip-flop, it suffers from clock load on four transistors and elevated propagation delay, setup, and hold times. In contrast, our flip-flop demonstrates a 99.6% reduction in power and energy consumption compared to the TSPC flip-flop by Yuan and Svensson, even though the latter has higher setup and propagation delay values. Notably, the proposed flip-flop eliminates clock skew issues arising from variations in wire usage or load capacitances. Through this comprehensive analysis, our proposed flip-flop emerges as more efficient in terms of energy, power consumption, propagation delay, setup, and hold time.

The outcomes of the simulation demonstrate that the suggested D flip-flop[2] exhibits reduced power consumption, a smaller footprint (in terms of the number of transistors), diminished clock load, shorter setup time, lower hold time, and a decreased clock-to-output propagation delay in comparison to currently available flip-flops. Although the setup time of the proposed flip-flop matches that of the NAND logic flip-flop, the latter incurs higher hold time, clock-to-output delay, and total transistor count, leading to increased power consumption.

TABLE IV. Comparison of existing Flip-flops with proposed flip-flop[2]

Type	t_{Setup} (sec)	t_{hold} (sec)	t_{Pc-q} (sec)	Clock load	Transistor count	Power (μw)	Energy (pJ)
Nand logic flipflop	4.00E-13	1.00E-12	1.1652E-12	2	26	**161.16**	**16.116**
TG logic MUX flipflop	6.00E-13	1.00E-12	8.9180E-13	8	22	**26.872**	**2.687**
C^2MOS flipflop	4.600E-11	4.00E-11	3.2014E-11	4	10	**0.0479**	**0.0048**
TSPC flipflop	5.00E-13	1.00E-13	5.3444E-13	4	11	**7.5947**	**0.759**
Proposed flipflop	4.00E-13	1.00E-13	2.5205E-13	2	10	**0.03027**	**0.003**

Table V presents a comparison of leakage power involving the proposed D flip-flop[1] and contemporary CNTFET-based alternatives across various combinations of data and clock. The results depicted in Table IV highlight the exceptional performance of the proposed flip-flop, outperforming other designs on average across different data and clock scenarios. This superiority is attributed to the lower leakage power exhibited by the proposed flip-flop compared to its counterparts. The flip-flop's design is both innovative and straightforward, featuring only two pVSCNTs and three nVSCNTs, enhancing the feasibility of fabrication. Notably, the average power consumption of the proposed flip-flop is impressively low, a crucial factor for practical applications. Additionally, the reported flip-flop demonstrates minimal leakage current, distinguishing it as a unique and standout solution among its peers. The overall exceptional performance of the flip-flop is evident across almost all data and clock scenarios, as illustrated in the table.

[Data, Clock]	Leakage Power (nW)				
	Reference Circuits with Year and Reference				Proposed Circuit
	2019 [10]	2014 [11]	2005 [12]	2001 [13]	
[0, 0]	27.169 × 10^3	9.584 × 10^3	0.776	797	3.231
[0, 1]	7.036 × 10^3	84.167 × 10^3	66.66	376	2.061
[1, 0]	5.832 × 10^3	9.714 × 10^3	18.58	248	1.45
[1, 1]	119.586 × 10^3	9.702 × 10^3	93.321	11.101 × 10^3	34.48
Average	39.905 × 10^3	28.291 × 10^3	44.834	3.13 × 10^3	10.306

TABLE V. comparison of leakage power of the proposed d flip flop with contemporary works[1]

IX. Conclusion:

In conclusion, the integration of novel approaches from the reviewed papers underscores the significance of combining methods to reduce the power consumption of D flip-flops. The first study introduces a unique flip-flop design utilising CNTFETs with a minimal transistor count, while the second study addresses leakage power in CNTFET-based circuits, highlighting the outstanding efficiency of the proposed design by introducing an energy efficient D Flip-flop by cascading the positive and negative TSPC latches using Stanford CNTFET model. The synthesis of these methods suggests a promising direction for achieving enhanced energy efficiency in D flip-flops. By leveraging the strengths of each approach, there is potential to create more robust, compact, and energy-efficient devices, thereby contributing to the ongoing evolution of low-power digital circuits in nanoscale applications.

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