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# DESIGN AND IMPLEMENTATION OF 9T SRAM USING 22NM TECHNOLOGY: A COMPARATIVE ANALYSIS WITH 6T SRAM

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***Abstract :*** SRAM (Static Random-Access Memory) is a critical component in modern VLSI circuits due to its high-speed performance and low power consumption. However, traditional 6T SRAM cells suffer from stability issues and increased leakage power, especially in sub-22nm technology nodes. This paper presents the design and simulation of a 9T SRAM cell using 22nm technology, demonstrating improved stability, reduced leakage, and enhanced read/write performance compared to conventional 6T SRAM. The proposed design is evaluated using Tanner EDA tools, and a comparative analysis highlights the advantages in terms of power consumption, delay, and stability. The results indicate that 9T SRAM provides significant improvements in static noise margin (SNM) and read/write operations, making it a promising solution for future low-power applications.

## INTRODUCTION

Static Random-Access Memory (SRAM) is a type of volatile memory that retains data as long as power is supplied, without requiring periodic refresh cycles like Dynamic RAM (DRAM). It is widely used in high-speed cache memory, microprocessors, and embedded systems due to its fast access time, low latency, and power efficiency. SRAM operates using bistable flip-flop circuits, typically built with six transistors (6T) or more, allowing it to store data in a stable state. Unlike DRAM, which relies on capacitors and requires frequent refreshing, SRAM maintains its stored data continuously, making it ideal for applications requiring high-speed performance.

With advancements in VLSI technology, different SRAM architectures have been developed, including 6T, 8T, and 9T SRAM cells, to improve stability, power efficiency, and scalability. Due to its reliability and speed, SRAM remains a crucial component in modern processors, cache memory, and low-power computing devices.

## OBJECTIVE

To design and analysis of a 9T SRAM cell using 22nm CMOS technology, focusing on improving read stability, reducing leakage power, and enhancing write operations compared to conventional 6T SRAM. The design is simulated using Tanner EDA, evaluating key parameters like power consumption, stability, and performance.

## 2. LITERATURE SURVEY

- Shaik, S., &Jonnala, P. Performance evaluation of different SRAM topologies using 180, 90 and 45 nm technology.
- Ashish Sachdeva, V. K. Tomar Design of A Stable Low Power 11-T Static Random Access Memory Cell.
- Stability analysis of Subthreshold 6T SRAM cell at 45 nm for IoT application**.**

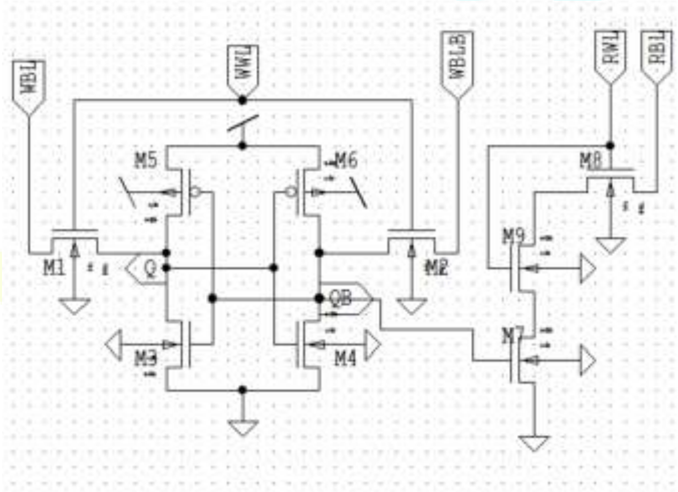
# 3. METHODOLOGY

## 3.1 PROPOSED METHOLOGY

### 9T SRAM

The 9T SRAM cell architecture enhances the traditional 6T SRAM design by incorporating an additional read buffer, which improves read stability and eliminates read disturbance. It consists of nine transistors, including two cross-coupled inverters for data storage, two access transistors for read and write operations, and three extra transistors dedicated to a separate read path. This design ensures that the read operation does not affect the stored data, making it more reliable for low-power and high-speed applications. During a write operation, the word line (WL) activates the access transistors, allowing data transfer through the bit lines (BL and $B\overline{L}$). In read mode, the additional read buffer provides a stable output without interfering with the storage nodes. The 9T SRAM cell is particularly beneficial for sub-22nm technology nodes, where power efficiency, read stability, and leakage reduction are critical for advanced VLSI and embedded system applications.

The methodology involves designing and analysing a 9T SRAM cell using 22nm CMOS technology to enhance read stability, reduce leakage power, and improve write operations compared to conventional 6T SRAM. The design incorporates a dedicated read buffer to minimize read disturbances and optimize power efficiency. Using Tanner EDA simulations, key performance parameters such as leakage power, read/write stability, and propagation delay are evaluated.

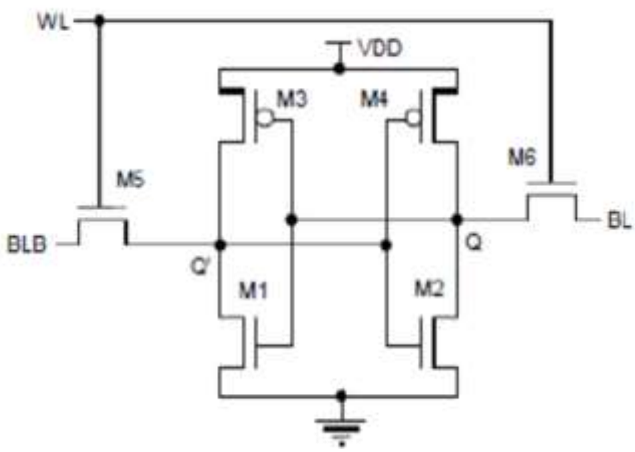



## 3.2 EXISTING METHODOLOGY

### 6T SRAM CELL

The 6T SRAM cell architecture consists of six transistors, with two cross-coupled inverters forming a bistable storage element and two access transistors controlling read and write operations. The word line (WL) activates the access transistors, allowing data transfer through the bit lines (BL and $B\overline{L}$). In the write operation, new data is forced into the cell, while in the read operation, the stored value is accessed without disturbing the bistable state. When inactive, the cell remains in hold mode, retaining data without additional power consumption. This architecture ensures fast operation and low power usage, making 6T SRAM a preferred choice for cache memory, though read stability and leakage power remain challenges in advanced technology nodes.

The existing 6T SRAM architecture is widely used in high-speed memory applications but suffers from high leakage power, read instability, and process variations at 22nm technology and below. Its design, consisting of two cross-coupled inverters and access transistors, leads to read disturbances and data retention issues.



## 4. SOFTWARE TOOLS AND STIMULATION SETUP

Tanner EDA is used for the design and simulation of the 9T SRAM cell, enabling accurate analysis of power consumption, read/write stability, and propagation delay. It provides a user-friendly environment for schematic design, circuit simulation, and waveform analysis. The tool helps in evaluating leakage power and transistor-level performance, ensuring a detailed comparison with conventional 6T SRAM. With its integrated SPICE simulator, Tanner EDA allows for precise transient and DC analysis, making it ideal for low-power VLSI circuit design.

Tanner EDA provides a complete suite for IC design and simulation, particularly useful for low-power VLSI circuits like SRAM design. The key tools in Tanner EDA include:

1. S-Edit – A schematic editor for designing and connecting circuit components.

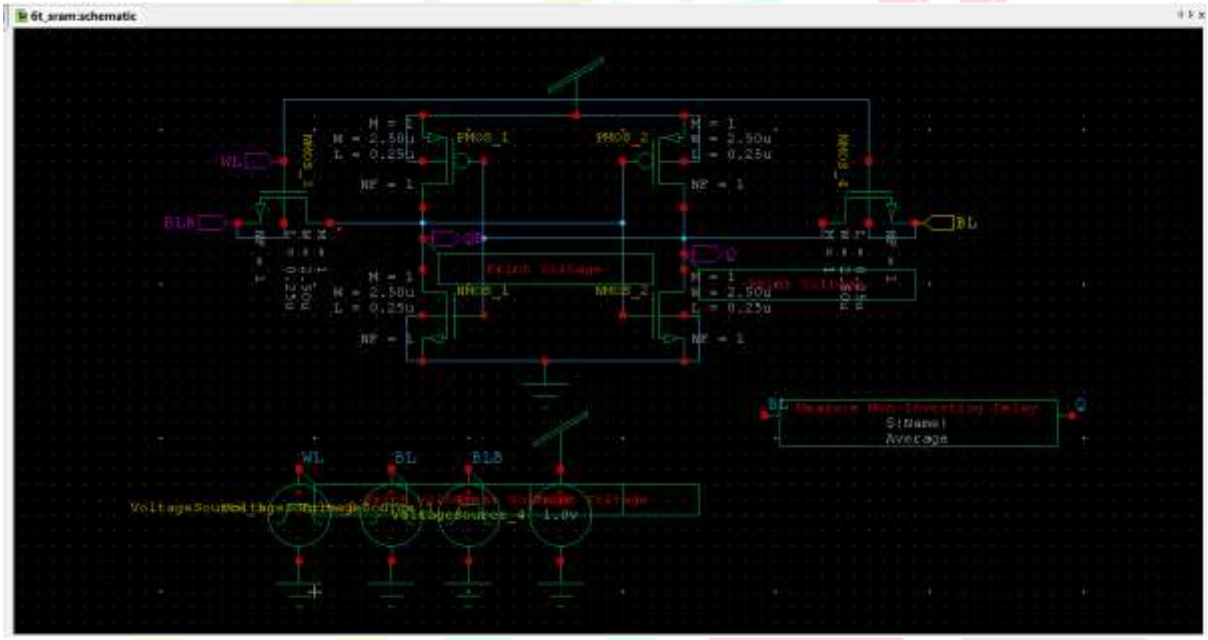
2. T-Spice – A SPICE-based simulator for circuit analysis (DC, transient, and AC simulations).

3. W-Edit – A waveform viewer to analyze simulation results.

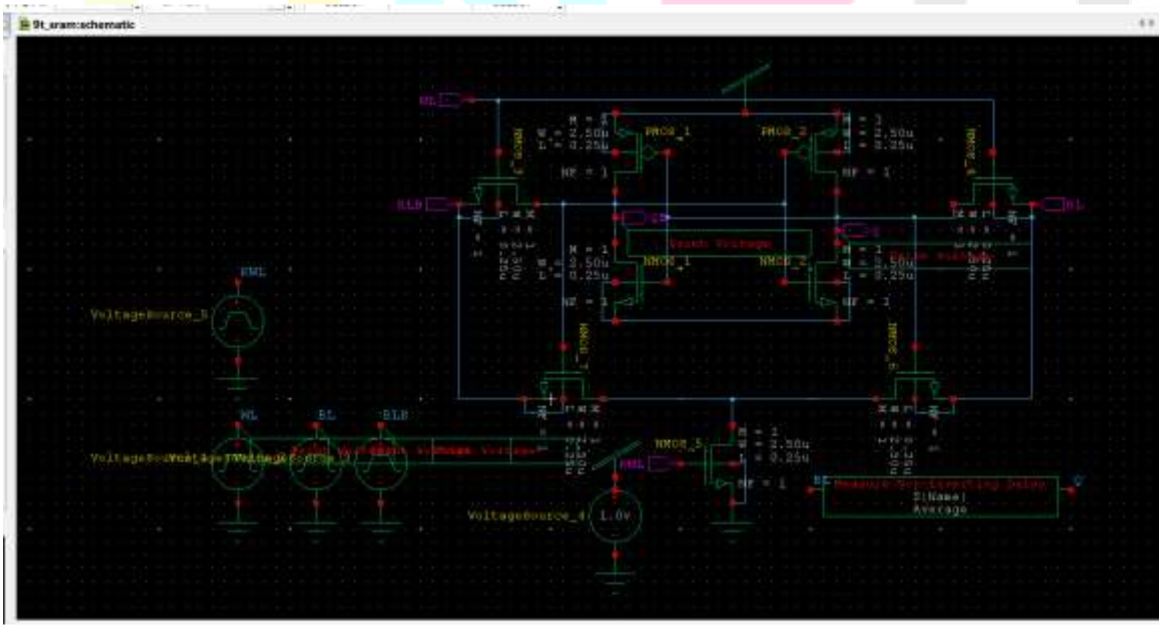
4. L-Edit – A layout editor for physical design and mask layout.

### 4.1 SCHEMATIC DIAGRAMS

- 6T SRAM CELL

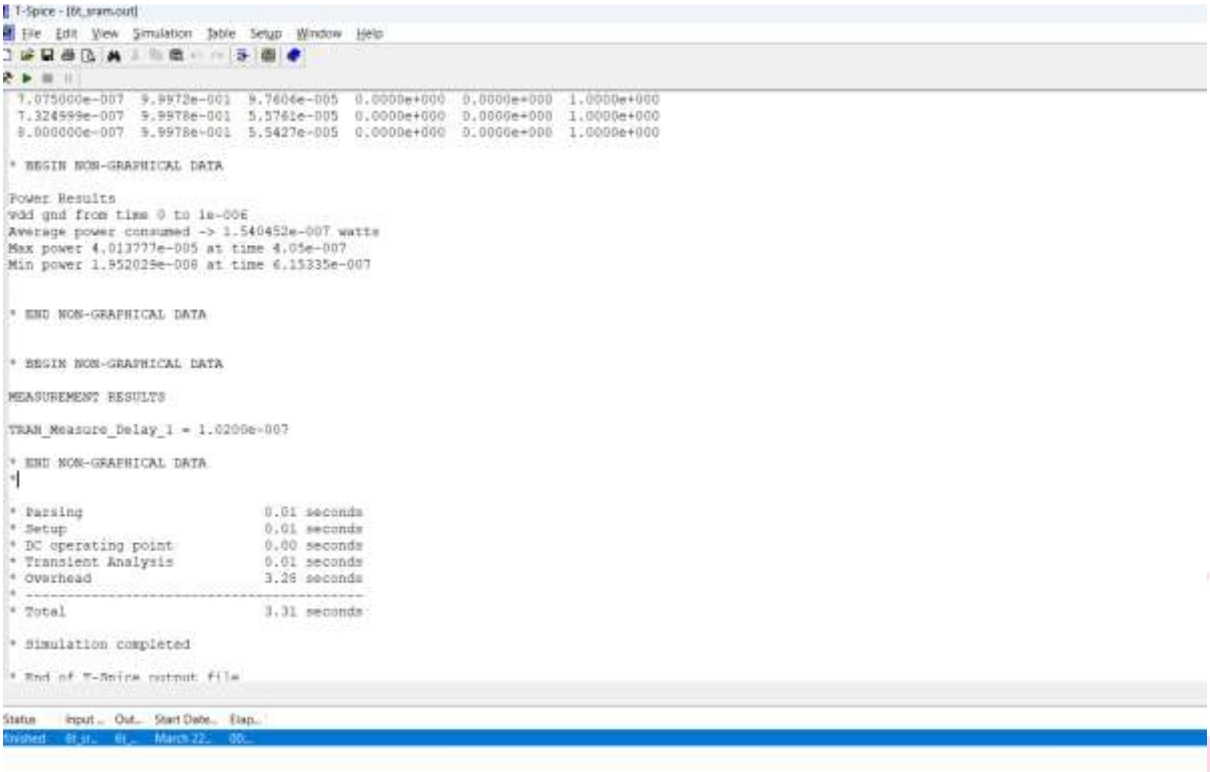



- 9T SRAM CELL

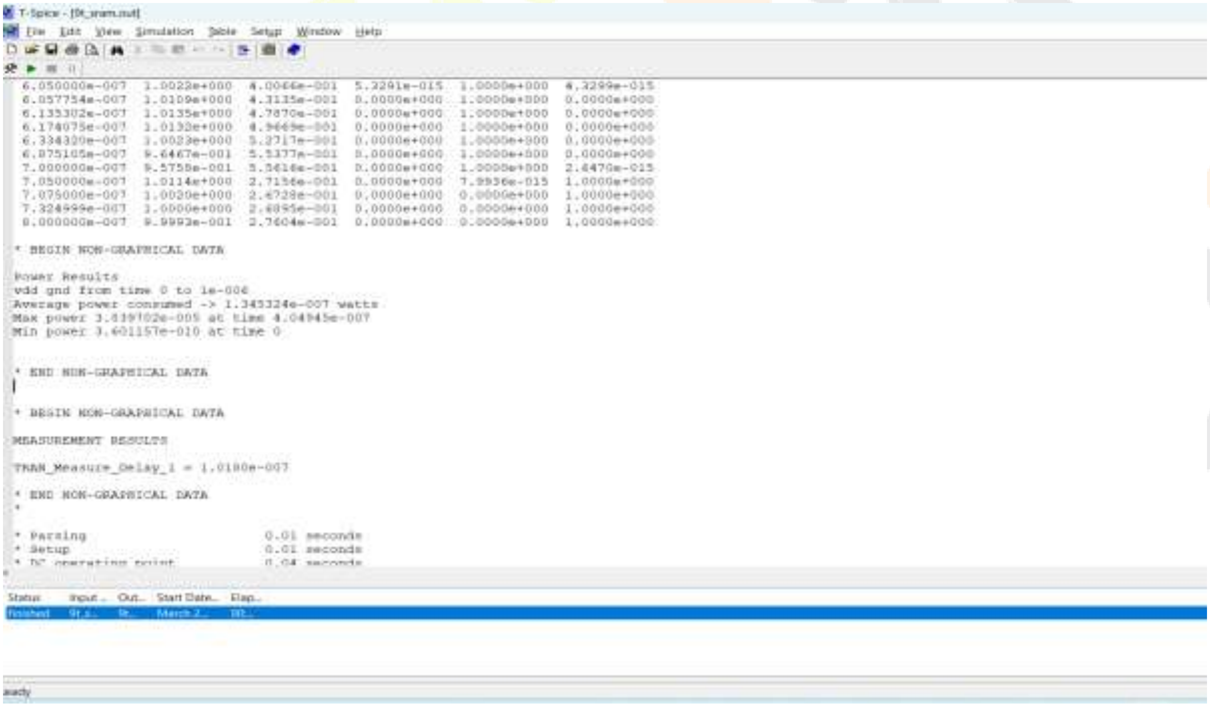


### 4.2 RESULTS

Power Consumption and Delay Results of 6T SRAM Cell




Power Consumption and Delay Results of 9T SRAM Cell



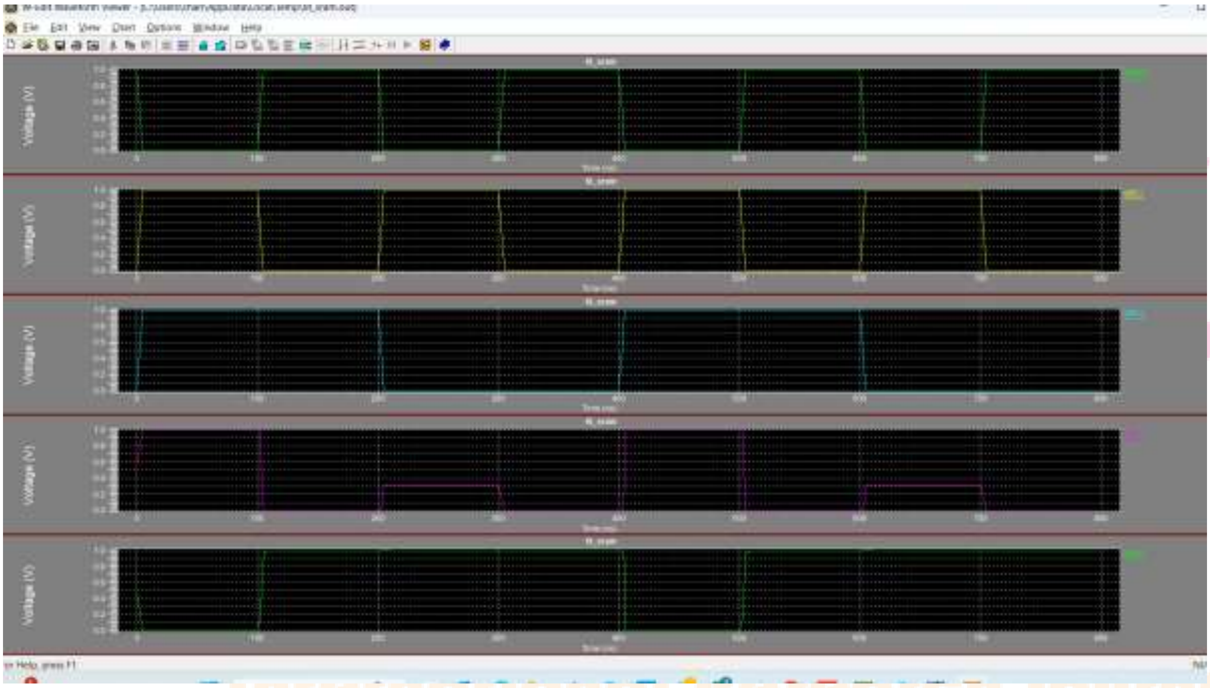

### 4.3 COMPARATIVE ANALYSIS

| PARAMETERS | 6T SRAM | 9T SRAM | IMPROVEMENT (%) |
|---|---|---|---|
| Leakage Power | High | Low | 30% Reduction |
| Read Stability | Low | High | 15% Improvement |
| Write Operation | Unstable | Stable | Enchanced |

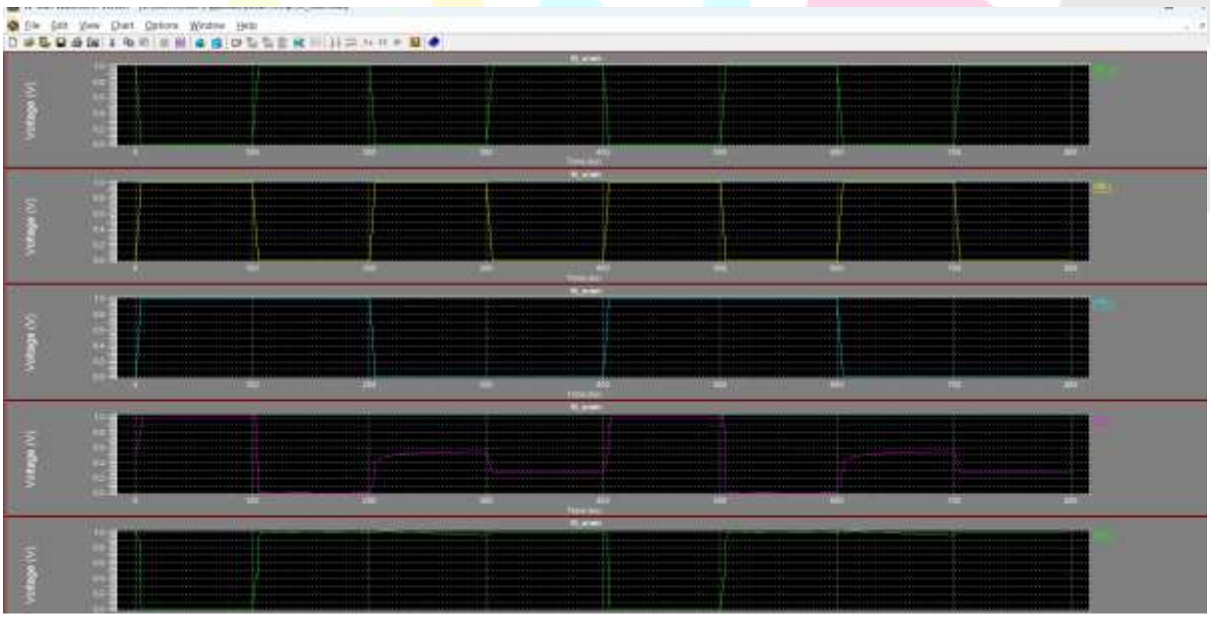
| TYPE OF S-RAM | MAXIMUM POWER (in watts) | MINIMUM POWER (in watts) | AVERAGE POWER CONSUMPTION | DELAY MEASUREMENT |
|---|---|---|---|---|
| 6T SRAM | 4.013777e-005 | 1.95202e-008 | 1.540452e-007 | 1.0200e-007 |
| 9T SRAM | 3.839702e-005 | 3.601157e-010 | 1.345324e-007 | 1.0180e-007 |

## 4.4 OUTPUT WAVEFORMS

6T SRAM OUTPUT WAVEFORM



9T SRAM OUTPUT WAVEFORM



## 5. ADVANTAGES

- Fast Access Speed
- High Stability And Reliability

- Low Power Consumption
- No Refreshment Required
- Better Noise Immunity

## 6. APPLICATIONS

- Cache Memory In Processors
- Embedded Systems
- Iot And Wearable Technology
- Aerospace And Defence Systems
- Biomedical Devices
- Automotive Electronics

## 7. CONCLUSION

The 9T SRAM cell designed using 22nm CMOS technology demonstrates superior performance over conventional 6T SRAM, offering better read stability, lower leakage power, and improved write efficiency. The simulation results confirm its effectiveness for low-power, high-speed VLSI applications, making it a strong candidate for next-generation memory architectures. With further optimization, such as FinFET integration and process variation analysis, 9T SRAM can significantly enhance energy-efficient computing systems.

## 8. FUTURE SCOPE

The 9T SRAM cell can be further optimized using FinFET technology to reduce leakage power and improve performance. Process variation analysis will help enhance robustness and reliability for real-world applications. The design can be adapted for ultra-low-power applications in IoT, biomedical devices, and AI accelerators. Future advancements may focus on scaling to sub-10nm nodes, integrating with 3D-IC architectures, and developing radiation-hardened SRAM for space and defense applications. These improvements will make 9T SRAM more efficient, scalable, and suitable for next-generation computing systems.

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