IJNRD.ORG ISSN : 2456-4184
INTERNATIONAL JOURNAL OF NOVEL RESEARCH AND DEVELOPMENT (IJNRD) | IJNRD.ORG
An International Open Access, Peer-reviewed, Refereed Journal

DESIGN AND IMPLEMENTATION OF SAMPLE AND HOLD CIRCUIT IN 180nm CMOS TECHNOLOGY

Mr.M Satyanarayana, K Srinath, E Srihitha, G Manasa

Assistant Professor, Dept of Electronics and Communication Engineering, TKR College of Engineering and Technology, Meerpet, Telangana

Students, Dept of Electronics and Communication Engineering, TKR College of Engineering and Technology, Meerpet, Telangana

Abstract :The project presents the implementation of error reduction techniques in sample and hold circuits(S/H). S/H suffers from the multiple errors such as aperture jitter, charge injection and clock feed through etc. Mainly two hold mode errors that is charge injection and aperture jitter. We are trying to mitigate these errors by using different design techniques. When a switch in the S/H turns on, the capacitor starts charging and discharges when it turns off. Due to this action the sampled output signal may suffers from attenuation that is called charge injection. Due to some overlap capacitance of gate and drain clock feed through error may also occur. This paper presents designing different S/H architectures to reduce these errors and also gives high gain, more stable, increased acquisition range, low power consumption. The proposed architectures are designed in 180nm CMOS Technology with input sinusoidal frequency 10MHZ and 1V Peak to peak. Sampling rate is 500MHZ. The design is target to gain of 65dB.

INTRODUCTION

In most analog to digital converters (ADC), the front end device is the sample and hold circuitry. Sample and Hold circuits are utilized to execute the sampling process on the analog input signal at a specific moment in an analog to digital converter.The sample and hold circuit can maintain the signal at that level for a designated time period,thus enabling repeated use of the signal during the conversion from analog to digital. Sample and Hold circuits are essential components in data conversion.

Conventional switched capacitor techniques leverage the excellent characteristics of capacitors and MOS switches, allowing for the implementation of various analog sample data circuits. It is an analog device that samples the continuously varying analog signal and retains its value at a constant level for a defined minimum duration.

S/H samples the continuously varying signal and retains it for a specific time duration. Within the S/H circuit, charge injection and clock feedthrough from the channel are the primary sources of errors when the switch is disengaged. The fact that the output value is internally used at slightly delayed moments does not impact the signal transfer characteristics since ultimately, the resulting value will correspond to the original sampling moment.

OBJECTIVE

To design a high speed, high-accuracy S/H circuit for 180nm CMOS technology.Main focus to improve circuit stability and robustness by minimizing the errors and to enhance noise immunity and rejection.The design is simulated using Tanner EDA, evaluating key parameters like power consumption, stability, and performance.

2. LITERATURE SURVEY

- Behzad Razavi,Design of sample and hold amplifiers for high speed low voltage A/D converters in 1997 using methodology, Switched-Capacitor sample and hold topology.
- National Semiconductor Corporation,Specification and architecture of sample and hold amplifier in 1998 using methodology,Switched-Capacitor sample and hold circuit using transmission gate switch technique.
- Amit Kumar Singh,Methodology for designing switched capacitor sample and hold circuit used in data converters in 2013 using methodology,Switched-capacitor sample and hold circuit with boostrap switch technique.

3. METHODOLOGY

3.1 PROPOSED METHOLOGY

The suggested S/H architecture includes a sampling switch, hold capacitor, a voltage follower at the input stage, and a unity gain buffer at the output stage. operational amplifier at the input stage and a unity gain buffer at the output stage. The sampling switch is activated by a positive CLK. Input is sampled at a frequency of 10MHz and 1V P-P. The S/H becomes active when it enters the saturation region, leading to a pinch-off situation and disconnection from the drain. If the drain of the sampling switch is linked to the hold capacitor, the drain will remain unaffected aside from the source junction. This is because it will experience charge injection. In sampling mode, the output value merely tracks the input value. In hold mode, the transistors connected to the output of the op-amp are switched off, even though they continue to operate in saturation. This will prevent charge injection in the channel from flowing into the op-amp's output. The op-amp will deactivate and its output will be maintained at high impedance, allowing the charge on the hold capacitor to be preserved Unity gain buffer which is connected at the output stage of the S/H circuit is always operational during both sample and hold mode and provides the voltage on hold capacitor to output of S/H circuit.

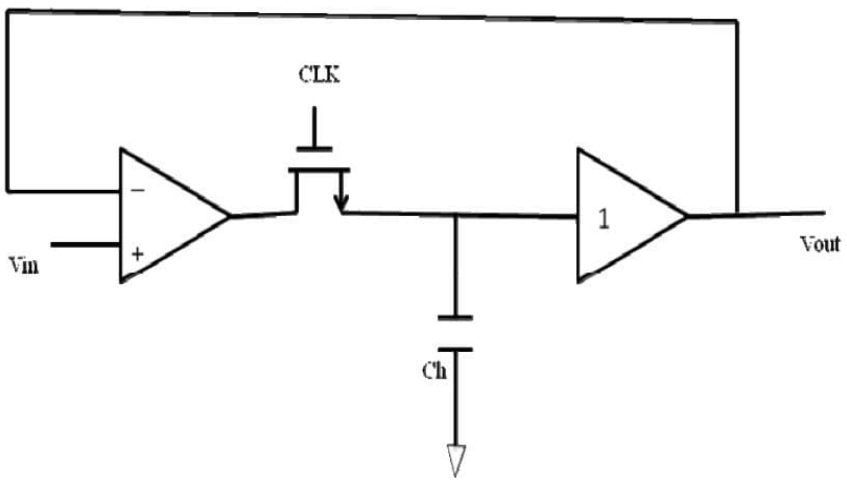


Fig 1.Proposed S/H Architecture

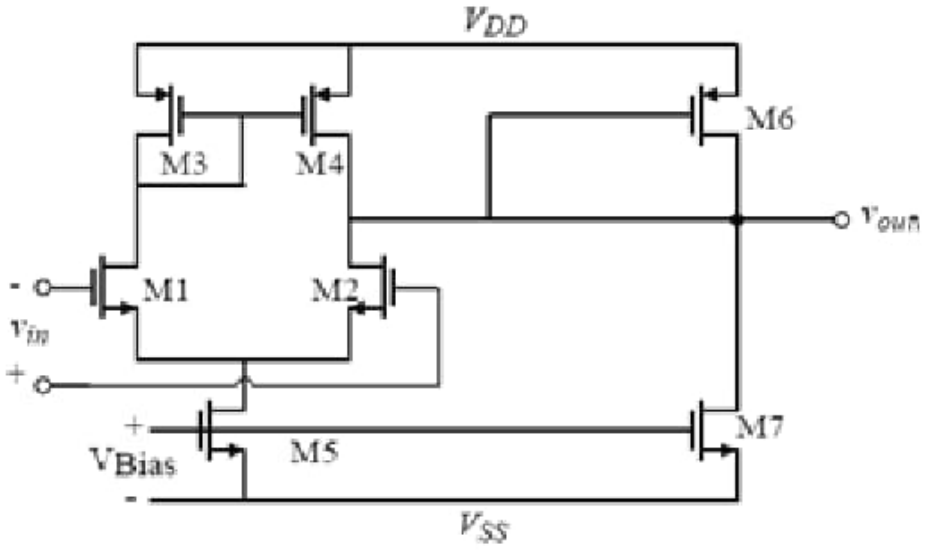


Fig 2. Two-stage op-amp construction

Working Principle:

➢ **Sampling phase (Track mode):**

- When the control signal (typically a clock pulse) is HIGH, the switch (usually a CMOS transmission gate) connects the input signal to the hold capacitor.
- During this phase, the capacitor charges (or discharges) to follow the instantaneous value of the input signal.
- The time constant of the charging/discharging process is determined by the ON-resistance of the switch and the capacitance of the hold capacitor. For the accurate sampling the time constant needs to be sufficiently small compared to the rate of change of the input signal.

➢ **Hold phase:**

- When the control signal transitions LOW, the switch opens, isolating the hold capacitor from the input signal.
- Ideally, the charge stored on the capacitor remains constant during this phase, "holding" the sample value of the input signal at the instant the switch opened.
- In reality, there will be some charge leakage from the capacitor through the OFF-resistance of the switch, the input impedance of the output buffer (if used), and any parasitic leakage paths. This leakage causes a gradual voltage droop or drift on the held value.

3.2 EXISTING METHODOLOGY

BASIC SAMPLE AND HOLD CIRCUIT

The sample and hold consists of a single CMOS switch and a hold capacitor and its works in two modes. They are sample mode and hold mode. M1 and Ch are the sampling switch and the hold capacitor. Whenever clock goes high M1 switch will turn ON which interns allows output voltage to track the continuous analog input signal. This is sampling mode. In the hold mode the signal value is fixed at its value at the moment of opening the switch. When clock goes low, M1 switch turns Off and Ch will keep output voltage equal to the value of input voltage. Sampling can be done in two methods which are series sampling and parallel sampling. Here we refer parallel sampling because the hold capacitor is in parallel with the signal. In series sampling hold capacitor will be connected in series.

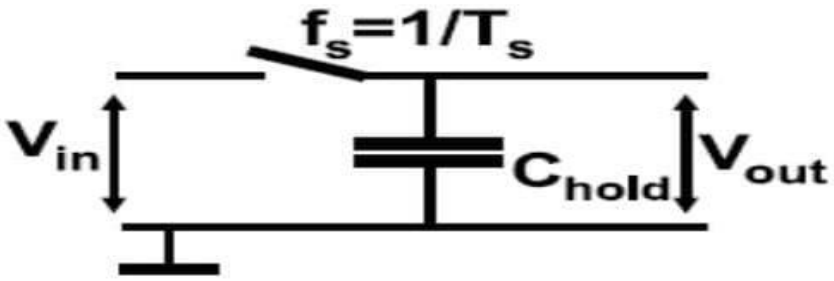


Fig 3.Basic CMOS sample and hold circuit

- Bootstrapped switch S/H:

  This technique aims to reduce the ON-resistance variation of the MOS switch with the input voltage, thereby improving linearity and bandwidth. Bootstrap capacitor is used to drive the gate voltage by an amount related to the input signal.

4. SOFTWARE TOOLS AND STIMULATION SETUP

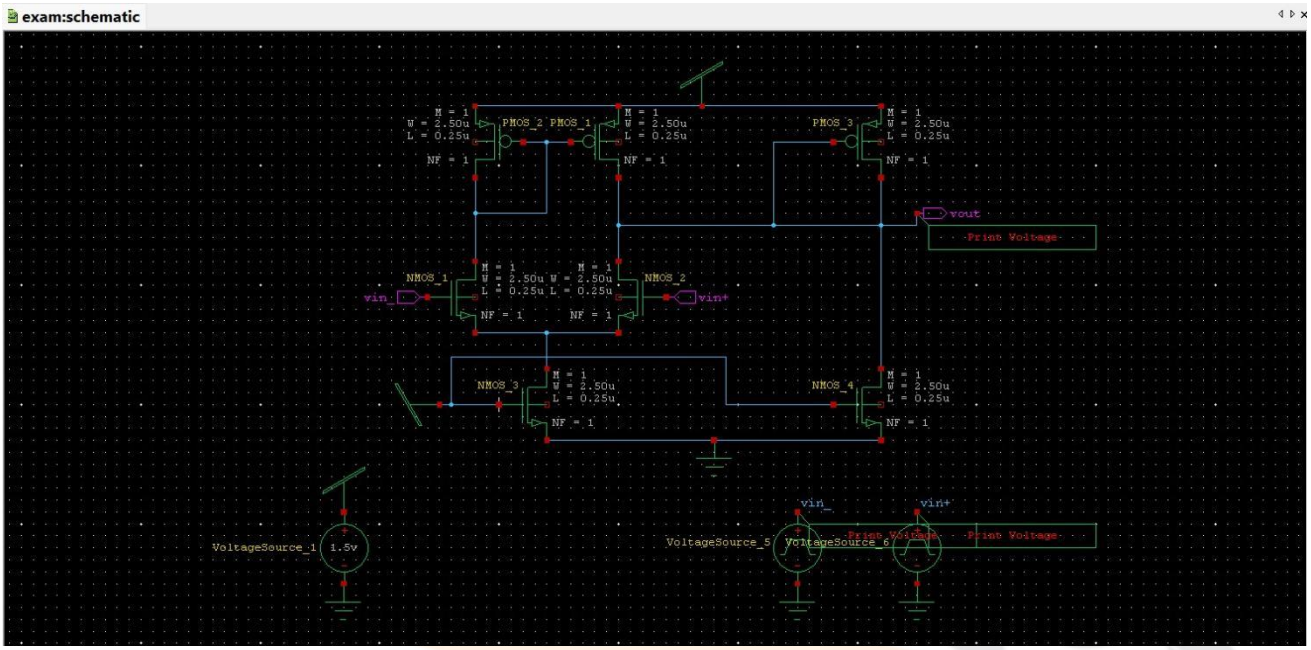
Tanner EDA is used for the design and implementation of sample and hold circuit in 180nm CMOS technology,to design a high speed, high-accuracy, to improve circuit stability and robustness by minimizing the errors and to enhance noise immunity and rejection. It provide a user friendly environment for schematic, circuit simulation, and waveform analysis.The tool helps in reducing errors and improve stablility. With its integrated SPICE simulator, Tanner EDA allows for precise transient and DC analysis, making it ideal for low-power VLSI circuit design.

Tanner EDA provides a complete suite for IC design and simulation, particularly useful for low-power VLSI circuits like SRAM design. The key tools in Tanner EDA include:

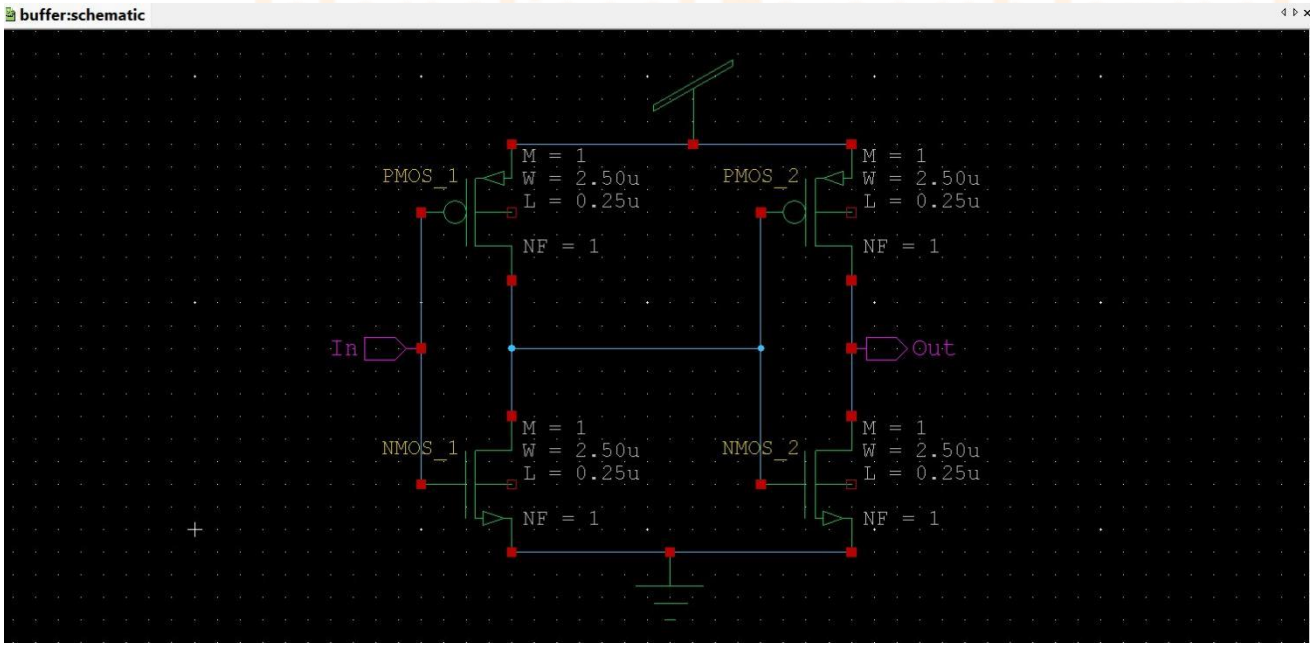
1. S-Edit – A schematic editor for designing and connecting circuit components.
2. T-Spice – A SPICE-based simulator for circuit analysis (DC, transient, and AC simulations).
3. W-Edit – A waveform viewer to analyze simulation results.
4. L-Edit – A layout editor for physical design and mask layout.

4.1 SCHEMATIC DIAGRAMS

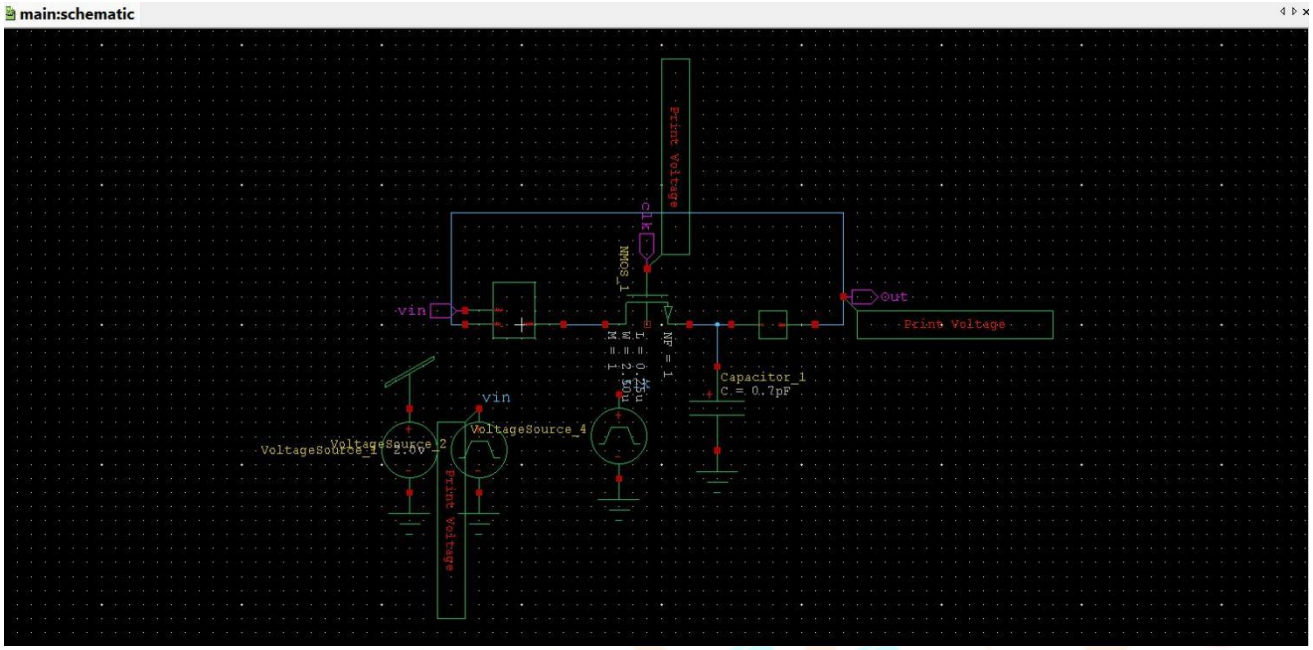
- **OPERATIONAL AMPLIFIER SCHEMATIC**



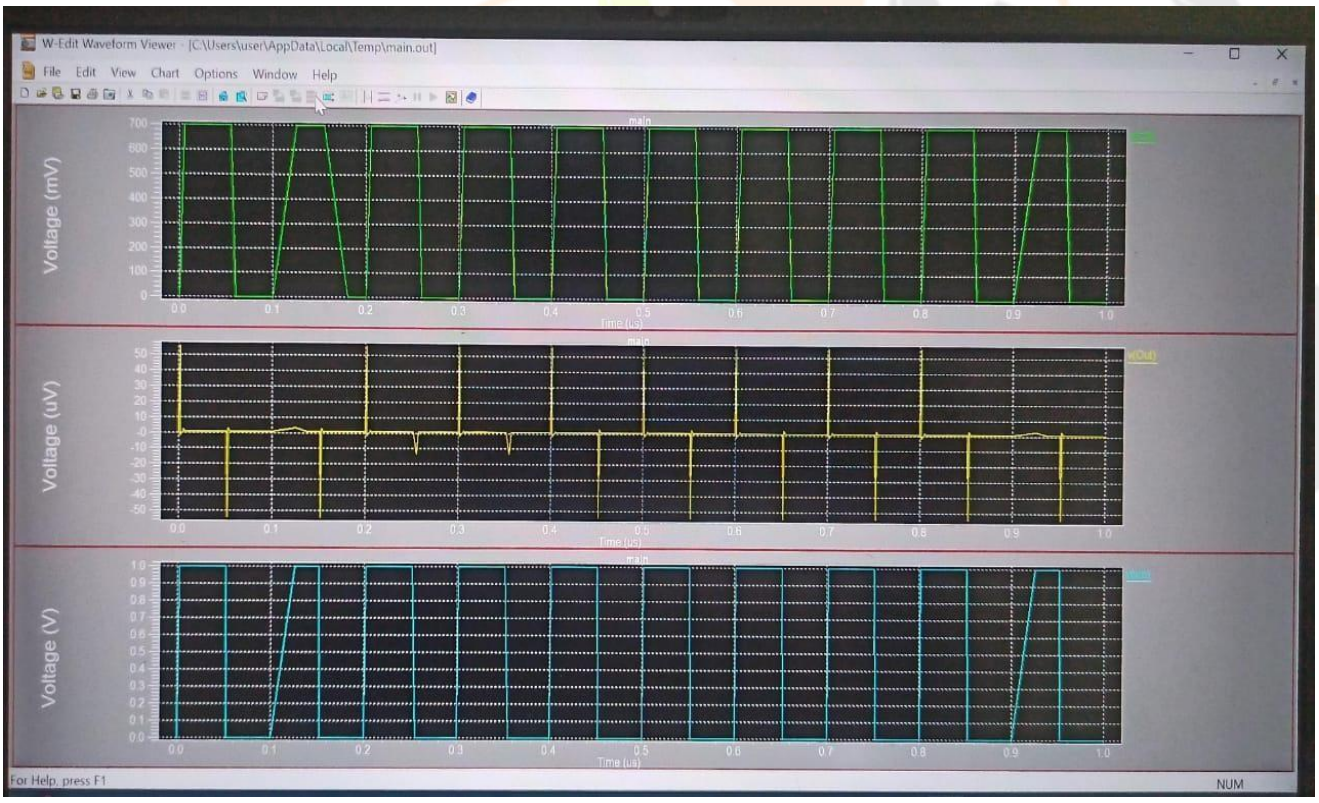
- **BUFFER SCHEMATIC**



- **SAMPLE AND HOLD CIRCUIT SCHEMATIC**



4.2. RESULTS



5. ADVANTAGES

- Low Power Consumption
- Reduced errors
- Advancement in S/H design techniques
- Increased gain.

6. APPLICATIONS

- In ADC applications
- High-Speed Data Acquisition Systems
- Advanced Sensor Interfaces
- Precision Instrumentation

7. CONCLUSION

This project successfully demonstrated the design and implementation of a sample a hold (S/H) circuit using 180nm CMOS technology. Through careful consideration of various design parameters and trade-offs, a functional S/H circuit was realized that met the desired specifications for acquisition time, hold droop rate, and power consumption within the constraints of the chosen technology node. The simulation results validated the theoretical analysis and confirmed the circuit's ability to accurately sample an input signal during the sampling phase and hold the sampled voltage with minimal degradation during the hold phase. The impact of key design choices, such as the size of the sampling switch and the hold capacitor, on the circuit's performance metrics was thoroughly investigated and optimized. Furthermore, the design process highlighted the inherent limitations and challenges associated with implementing analog circuits in nanoscale CMOS technologies, particularly concerning leakage currents and parasitic capacitances.

In conclusion, this project provides a practical understanding of the design principles and implementation considerations for sample and hold circuits in modern CMOS technology. The findings contribute to the knowledge base for analog and mixed signal circuit design and serve as a foundation for further exploration and optimization of high-performance data acquisition systems. Future work could focus on exploring techniques to further reduce power consumption, improve linearity, and enhance the hold accuracy of the S/H circuit in the 180nm CMOS process.

8. FUTURE SCOPE

The proposed S/H architectures have shown considerable improvements in reducing charge injection and clock feedthrough errors. Future developments can leverage more advanced CMOS nodes such as 65nm or 28nm to reduce parasitic effects and improve speed and power efficiency. Incorporating adaptive switching techniques or machine-learning-based calibration mechanisms may further enhance performance under process, voltage, and temperature variations. Moreover, exploring time-interleaved S/H structures can support higher sampling rates suited for ultra-high-speed ADCs. Integration into full system-on-chip (SoC) designs for applications such as RF front-ends, high-resolution imaging systems, and biomedical signal acquisition could provide valuable real-world validation. Additionally, continued innovation in layout optimization and switch control strategies will help push the performance boundaries of future S/H circuits**.**

9. REFERENCE

1. Methodology for designing switched capacitor switched capacitor sample and hold circuit used in data converters" IET circuits, device and systems,28th Nov 2013.
2. Biao Li, "A high DC gain op-Amp for sample and hold circuit", proceedings of the 2nd international conference on computer science and electronics engineering, ICCSET 2013.

3. Yan Xiang, Fan xianginning, “Design of sample and hold circuit for a re-configurable ADC”, international conference on computer science and service system, 2012 southeast university, Nanjing, China.
4. Specification and architecture of sample and hold amplifier, national semiconductor corporation, July 1998.
5. Behzad Razavi, “Design of sample and hold amplifiers for high-speed low voltage A/D converter”, custom integrated circuit conference, IEEE 1997.
6. “Analog integrated circuit design” by David, A. Johns and Ken Martin.
7. “CMOS Analog circuit design” by Philip E. Allen and Douglas, R. Holberg.
8. “Data conversion Engineering” by Richard,H.Baker.