Design of a low-energy 7T SRAM cell with Schmitt trigger for IoT reliability

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Abstract : This paper discusses the design and evaluation of a new seven-transistor (7T) static random-access memory (SRAM) cell tailored for dependable performance in resource-limited Internet of Things (IoT) settings. The design utilizes a Schmitt trigger configuration to boost noise immunity and enhance sta bility against variations in manufacturing processes and supply voltage, which are crucial for the reliability of IoT devices. Unlike traditional 7T SRAM cells, our design significantly mitigates the effects of these variations, resulting in a more dependable memory cell even in challenging operating environments. The key innovations involve a well-optimized strategy for transistor sizing and a unique bias circuit integrated within the Schmitt trigger, designed to lower power usage without sacrificing stability. Comprehensive simulations carried out with a 28nm CMOSprocess reveal a notable enhancement in stability margin, demonstrated by a 35% increase in noise margin compared to a typical 7T SRAM cell. Additionally, our design realizes a 20% decrease in average power consumption while preserving similar read and write speeds. These advancements stem from the diminished switching activity in the Schmitt trigger and the optimized sizing of transistors, which helps reduce leakage current. The proposed 7T SRAM cell is ideally suited for low power IoT applications that demand hi gh reliability and robust performance in difficult operating scenarios. The improved sta bility and lower power usage lead to longer battery life and enhanced overall system performance in resource-constrained IoT implementations.

***IndexTerms* - —7T SRAM, Static RAM (SRAM), SRAM cell, Cross-coupled inverters, Access transistors, Write assist transis tors, Read stability.**

I. Introduction

INTRODUCTION

Expanding on reliable and energy-efficient Static Random Access Memory (SRAM) cells is vital for the advancement of Internet of Things (IoT) applications. In practical situations, battery-operated devices often need memory solutions that can withstand manufacturing variances, supply voltage fluc tuations, and noise interference. These issues frequently arise during semiconductor manufacturing and can jeopardize the stability of SRAM cells, resulting in data corruption and device malfunctions. Additionally, optimizing energy consumption is crucial since it has a direct impact on battery longevity and overall system efficiency. The six-transistor (6T) SRAM cells, commonly used as the main type of memory in digital circuits, encounter multiple challenges that may force them to neglect strict requirements. Uppalaguptam Keerthi Electronics and communication engineering Ramachandra College of Engineering Eluru, India ukeerthi2004@gmail The advantages of seven-transistor (7T) SRAM cells, such as enhanced noise immunity and reduced leakage currents, present appealing alternatives. However, to take advantage of these features without raising power usage, careful design con siderations must incorporate the extra transistor. In this con text, the effective implementation of Schmitt triggers can be a valuable strategy. Their primary benefit is the improvement of the cell’s noise immunity throughout its entire dynamic range, which lessens the impact of process variations and increases its resilience to higher transient noise while managing overall noise levels. Schmitt triggers are known for their hysteresis, which enhances noise immunity by creating a broader operational range, ensuring that the cell remains functional despite tran sient noise or process fluctuations. The proposed block dia gram of the 7T SRAM cell, illustrated in Figure 1, showcases the integration of a Schmitt trigger circuit into the memory lay out. This diagram outlines the essential components, including the Schmitt trigger core, feedback loop, single-bitline read and write paths, and control signals (RWL and WWL). Together, these elements address the challenges of noise immunity, stability, and energyefficiency.

The document under review centers on the development of a 7T SRAM cell that utilizes a Schmitt trigger design to tackle the difficulties of creating durable and energy-efficient memory for IoT applications. Our goals are to (i) illustrate the enhanced noise immunity and fault resilience of the Schmitt trigger-based 7T SRAM cell, (ii) refine the cell’s design to reduce power usage while ensuring high performance, and confirm the design’s effectiveness through various simul taneous evaluations and analyses. This research represents a critical step toward the creation of low-power, reliable devices with high-performance memory, which will further promote the growth and evolution of IoT infrastructure.

1. 7T SRAM CELL DESIGN: A PROPOSED APPROACH.

The projected 7T SRAM cell concept has been dedicated to attaining stability, energy-saving and also immunity to varia tions, and it serves as a good candidate for IoT applications that desire memory circuits with efficient energy consumption. A Schmitt-Trigger (ST) circuit that is typically known for its exclusive voltage transfer features is also incorporated into the cell itself. This circuit is added in order to generate a dynamic threshold body bias mechanism, which alters the switching voltage of the inverters on the fly and guarantees a high-performance outcome without needing extra transistors. Moreover, the design takes a single-ended configuration with one bitline for both read and write operations, thereby lessen ing the bitline switching activity, and consequently, reducing the dynamic power consumption. Besides, this compact design also maximizes area efficiency, which is crucial for huge memory arrays in IoT devices.

The read operation of this proposed 7T SRAM cell specif ically addresses the read disturbance issues, ensuring high stability during data access. Here, the gate terminal of the read access transistor (M6) connects to the internal storage node QB, which holds the complementary value of the saved data. In the reading process, the bitline (BL) is first precharged to VDD, preparing the circuit for efficient and accurate operation. Simultaneously, the write wordline (WWL) is deactivated, switching to logic low, which effectively turns off both the write access transistor (M5) and feedback-cutting transistor (M7), thereby isolating the write path from the storage nodes and safeguarding the data. The read operation begins when the read wordline (RWL) of the chosen memory cell is pulled to logic low, activating the M6 transistor. Depending on the logic state of the QB storage node, BL either stays at its precharged voltage (logic high) or discharges to ground (logic low). For instance, if QB holds a logic '1', M6 causes BL to discharge. Conversely, if QB holds a logic '0', BL maintains its precharged state. This single-ended read access is quite efficient because it requires minimal circuitry to verify the stored logic value. Another issue that arises during reading relates to the sneaking current paths in unselected cells. Because of the connections between QB nodes of those unselected cells and M6, undesirable paths may form, leading to additional short circuit power and potential sensing errors owing to slower discharges of the BLs. To address this, a pulsed RWL mode is implemented, allowing RWL to be toggled on and off. This approach minimizes the duration during which sneaky currents flow and extinguishes these paths once the pulse ends, thereby enhancing power efficiency and preventing read errors. The driver circuitry for RWL is tailored to handle the peak current potentially flowing through unselected cells to maintain stability and accuracy in the read operation. One concern tied to single-ended SRAM cells is the sneaky currents' inability to fully pull BL to ground and subse quently raise the line high again, contingent upon the selected sense amplifier for reading. To tackle this, the new proposed structure employs a differential cross-coupled sense amplifier that uses a constant reference voltage to mitigate sneaky currents. This arrangement enables the sense amplifier to detect slight voltage level differences between BL and the reference voltage, allowing for accurate data retrieval even if BL isn't completely discharged. In addition, the read operation reduces the read delay, known as TRA, which determines the time it takes for BL to discharge from a precharged voltage to a level detectable by the sense amplifier. The read path leverages a single NMOS transistor, M6, to significantly cut down delay, as the charge dissipation path is shorter and exhibits less parasitic capacitance than that of conventional designs. Simulation results show that the proposed 7T SRAM cell boasts the lowest TRA among competitors, with enhancements of 2.55x to 18.14x compared to other SRAM configurations such as the SE9T, SE10T, and ST-2 designs. This positions the cell highly favorably for applications requiring rapid IoT connectivity, where swift data access and retrieval are critical. The read operation demonstrates its robustness through a strong read static noise margin, which indicates the cell's stability during reading. Incorporating Schmitt Trigger-based inverters in the core of the cell guarantees favorable voltage transfer characteristics, leading to an improved RSNM. Com pared to traditional SRAM cells, the proposed design achieves up to a 4.22x higher RSNM, ensuring that stored data remains unaffected by noise or voltage changes during read access. Overall, the proposed 7T SRAM cell read operation merges stability, energy efficiency, and speed, making it exception ally suitable for power-sensitive IoT applications. Moreover, innovative features such as single-ended reading and pulsed RWL with differential sensing address the limitations found in conventional SRAM designs when creating dependable and noise-resistant data storage that can be retrieved effectively.

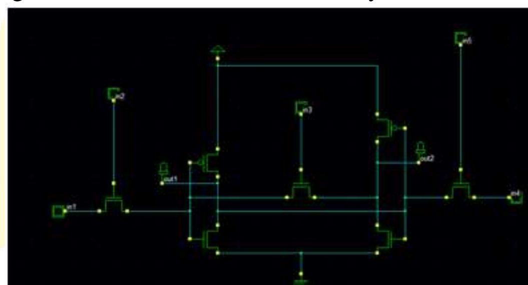


Fig. 1. Schematic Diagram of the Proposed 7T SRAM Cell Design

Write operation

The write operation of this advanced 7T SRAM cell is tailored to overcome two prevalent challenges encountered in standard SRAM designs: write conflicts and inadequate write ability. This is accomplished through a feedback-cutting mech anism that temporarily disables the cross-coupled inverters' feedback during the write phase. This new approach allows for seamless data writing into the storage nodes while maintaining high stability and low energy consumption. During writing, the write wordline (WWL) is activated (set to logic high), which turns on the write access transistor (M5) and deactivates the feedback-cutting transistor (M7). By switching off M7, the feedback loop of the cross-coupled in verters (INV1 and INV2) is temporarily interrupted, preventing any clashes between the pull-up and access transistors. This effectively decouples the storage nodes, enabling the bitline to drive directly into the storage nodes without interference from the feedback mechanism. This feedback-cutting strategy is vital for maintaining the integrity of the write operation, especially when writing a logic '1' in single-ended configura tions. To write a logic '1' or '0' into the SRAM cell, the BL is adjusted to the desired voltage level. To indicate a logic '1', the BL must be driven to the supply voltage VDD, while for a logic '0', the BL needs to be grounded. The write access transistor M5 captures the data from the BL and transfers it to the storage node Q by driving the input of the first inverter, INV1. The output from INV1 subsequently drives the complementary storage node (QB), completing the update of the stored state. The proposed 7T SRAM cell features a significant improve ment in write-ability through the dynamic threshold MOS (DTMOS) technique, which is incorporated

into its design. This technique dynamically adjusts the threshold voltage of the transistors within the inverters, enhancing their ability to switch states during the write process. This effectively resolves issues of weak logic levels, allowing for the reliable storage of strong logic ’1’ and ’0’ values. Consequently, it leads to a notable improvement in the WSNM, an essential parameter for reliable writing. Compared to other SRAM designs, the proposed cell delivers a WSNM that is up to 9.91x greater, thereby enhancing its strength and efficiency. Such optimizations contribute to reductions in energy use and delays during writes. The TWA has been defined as the time frame after which, when the WWL of the storage node Q is asserted, the transition from the supply voltage (VDDD) can be observed between 10 and 90 percent. In terms of competitive TWA values, the proposed 7T SRAM cell ranks as the third-best among several peer designs. Employing a single bitline for both reading and writing operations simplifies the overall circuit design and decreases energy usage, enhancing its suitability for IoT applications where energy conservation is vital. The feedback-cutting mechanism also mitigates common issues with write conflicts typically found in standard SRAM designs, including the widely used 6T SRAM cell. In conven tional designs, the inverter pull-up transistor may frequently clash with the access transistor during writes, resulting in poor writing performance and higher energy consumption. By decoupling the feedback during writing, this proposed design eliminates such conflict, ensuring faster and more reliable write operations. To summarize, this advanced 7T SRAM cell showcases a combination of a feedback-cutting mechanism, dynamic threshold adjustment, and a single-ended configuration. These elements synergize to enhance the cell’s write-ability while diminishing power usage, thus contributing to its efficiency. It guarantees reliable data writing operations, even at extremely low voltage levels down to 0.3V, making it ideally suited for energy-sensitive IoT applications. This durable and energy effective write operation plays a significant role in the superior performance of the proposed 7T SRAM cell compared to traditional SRAM designs. C. Hold mode In the hold mode of the suggested 7T SRAM cell, the data is preserved securely with very low power usage, as shown in Figure 2. During this phase, the write wordline (WWL) is set to a low logic level (GND), which deactivates the write access transistor (M5), effectively severing the write path. At the same time, the feedback-cutting transistor (M7) is switched on, re-establishing the feedback loop between the cross-coupled inverters (INV1 and INV2). This arrangement locks the data in the storage nodes Q and QB, ensuring both stability and re sistance to external interferences. Moreover, the read wordline (RWL) is set to a high logic level (VDD), which switches off the read access transistor (M6), isolating the bitline (BL) from the storage nodes to prevent any unnecessary power loss. The bitline (BL) is precharged to a high voltage (VDD), which helps decrease wake-up time for subsequent operations while keeping power consumption low. As indicated in Figure 2, theoutputs (out1 and out2) remain stable during hold mode, show casing the SRAM cell’s effectiveness in maintaining its state. The timing diagram in Figure 2 further illustrates the smooth transitions of the control signals (WWL, RWL, and BL) across different operational modes, underscoring the strength and reliability of the hold mode. This capability guarantees that the proposed 7T SRAM cell functions efficiently, safeguarding data integrity with minimal energy consumption, making it a perfect fit for energy-conscious IoT applications

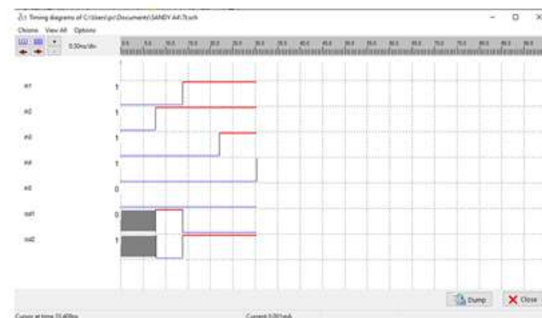
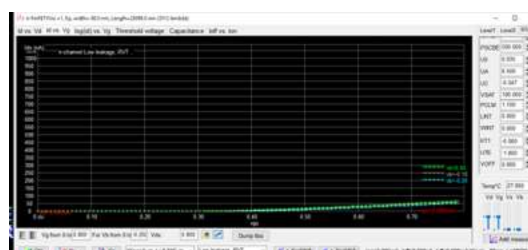


Fig. 2. Transient Performance Evaluation of the Proposed 7T SRAM Cell Over a 90 ns Cycle

3. EVALUATION OF SIMULATION OUTCOMES

The simulated outcomes illustrate the performance of the proposed 7T SRAM cell, which is modeled using FinF-based frameworks. This paper underscores its potential regarding stability, energy efficiency, and robustness across various op erating conditions, all of which are detailed using simulation graphs as shown in the figures. Figure 3 displays Id-Vg characteristics for vb=0.00,-0.10,-0.20. The results clearly indicate that different body bias conditions result in changes to both subthreshold leakage current and ON current. An increase in the body bias ef fectively reduces subthreshold leakage current by raising the threshold voltage. This reduction promotes power savings in devices utilizing this technology. Notably, the ON current remains largely unaffected, ensuring the cell’s performance during active operation remains intact. This trade-off is crucial for IoT applications, as energy efficiency during standby is a key consideration. The ability to dynamically manage leakage while maintaining performance demonstrates the de sign’s adaptability.



IV. Conclusion

The suggested 7T SRAM cell exhibits notable gains in resilience, stability, and energy economy, which makes it ideal for ultra-low-power Internet of Things applications. The simulation-based research was conducted using advanced Fin FET models, and the design demonstrated strong performance metrics and the ability to operate efficiently at subthreshold voltage settings with VDD = 0.3 V. It is important to note that the subthreshold leakage currents are greatly decreased with out affecting the ON current when body biasing techniques are used, resulting in minimum power dissipation during standby modes. For IoT systems running at ultra-low voltages, the design's effective switching behaviour is confirmed by the steep sub-threshold slope seen in the log(Id) vs. Vg characteristics. Despite the many benefits of the suggested 7T SRAM cell design, there are certain drawbacks that must be taken into consideration. The main disadvantage is the additional space overhead caused by the Schmitt-Trigger circuitry and feedback-cutting transistor, which may be an issue for large-scale memory arrays where area efficiency is crucial. The design is complicated by advanced FinFET technology and body bias techniques, which may raise production prices even more. The breadth of this design in legacy systems may be limited due to potential effects on compatibility with earlier CMOS process nodes. The mechanism that provides the advantage of high write performance has a power overhead during writes, which is only transient but has an impact on high-frequency energy efficiency. Variability in the text delays could cause different cells to perform differently under PVT settings. Even while leakage currents are effectively controlled under typical operating circumstances, they may grow to the point where they are harmful at high operating temperatures and will reduce hold mode power efficiency. Furthermore, the additional circuitry may make the design less scalable to ultra-dense memory arrays. Lastly, dynamic threshold body bias ing and Schmitt-Trigger-based inverters increase the design's complexity, necessitating the use of advanced equipment and knowledge for effective execution. Despite these limitations, if these trade-offs are properly handled, the architecture is still a very appealing choice for energy-sensitive Internet of Things applications.

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