DESIGN OF A HIGH-SPEED LOW-POWER CLOCK-GATED SYNCHRONOUS COUNTER

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Abstract : Synchronous counters are widely used in digital systems but often suffer from high power consumption due to unnecessary switching activity and leakage currents .A 45 nm CMOS clock-gated synchronous up/down counter is presented in this work. Local clock generators (LCGs) local clock pre-evaluators (LCPEs) and local clock selectors are all used in the suggested design. (LCSs) and Toggle Flip-Flops (TFFs) to cut down on needless clock switching. The Stacking Inverter and LECTOR (Leakage Control Transistor) techniques are used to reduce leakage power even more. the architecture of the counter. Cadence Virtuoso was used for both implementation and simulation of the design. The results of the simulation show a 5. 93 percent improvement in propagation delay and a 44. 38 percent reduction in power consumption. in contrast to the traditional synchronous counter. Low-power VLSI applications can benefit from the suggested counters enhanced performance and energy efficiency.

Keywords: **- Synchronous Up/Down Counter, Stacking Inverter, LECTOR, Low-Power VLSI**

I. INTRODUCTION

The advancement of modern electronic devices has increased the demand for digital circuits that can operate with high speed and low power consumption. Efficient hardware is necessary for gadgets like wearable technology mobile phones Internet of Things applications and portable embedded systems. to enhance overall performance and battery life. Counters are among the most important sequential circuits in digital communication systems because of their extensive use. timers signal processing units clocks and frequency dividers. Because all flipflops are simultaneously activated by a shared clock signal synchronous counters are typically preferred over asynchronous ones because they decrease latency and increase speed. receptacles. Nevertheless increased carry propagation delay and needless switching activity continue to be problems for conventional synchronous counters. which as the number of bits increases result in lower performance and increased power consumption. One widely used method for. Clock gating reduces pointless switching transitions. This work aims to study a CMOS clock-gated synchronous up/down counter in order to increase speed and power. The design uses a small toggle flip-flop structure and high-speed local clock generation to reduce delay. The proposed counter performs better removes pointless transitions and enhances the carry propagation mechanism. overall compared to conventional synchronous counter designs.

II. LITERATURE SURVEY

Synchronous counters are widely used in digital systems for timing, frequency division, control, and counting applications. With the increasing demand for portable and high-performance electronics, designing counters with low power consumption and high speed has become essential.Lee Joo and Kong [1] proposed a CMOS clock-gated synchronous up/down counter using a compact TFF structure and local clock generation techniques. The design employed Local Clock Generators (LCGs), Local Clock Pre-Evaluators (LCPEs), and Local Clock Selectors (LCSs) to reduce unnecessary clock transitions, resulting in higher operating speed and lower dynamic power consumption. However, leakage power reduction was not addressed.Kim et al. [2] presented a low-power synchronous counter with clock gating integrated into the carry propagation path. By activating local clocks only during state transitions, the design minimized switching activity and improved energy efficiency.Johnson, Somasekhar, and Roy [3] proposed an effective leakage reduction method based on transistor stacking. The technique substantially reduced standby power dissipation while maintaining acceptable circuit performance.The literature indicates that most existing works focus on reducing dynamic power through clock gating and improving speed through optimized counter architectures. However, leakage power remains a significant concern in modern CMOS technologies. Therefore, the proposed synchronous counter integrates LECTOR and stacking inverter techniques within a clock-gated architecture to reduce leakage power while maintaining high-speed operation and energy efficiency.

III. RESEARCH METHODOLOGY

A local clock generation method is used in the design of the suggested synchronous up/down counter. to attain low power consumption and high speed. The suggested architecture differs from traditional synchronous counters in that all flip-flops receive the same clock signal. only produces local clock pulses for the flip-flops that require state changes during a counting operation. Both needless switching activity and dynamic power dissipation are greatly decreased as a result. Local Clock Pre-Evaluators (LCPE) and Local Clock Selectors (LCS) are used for the higher-order counter sections. Before the actual carry signal is received from the source the LCPE analyzes the current counter states to forecast future carry conditions. section of lower order. By reducing carry propagation delay this carry pre-evaluation improves the counters overall operating speed. The LCS then receives the preevaluated carry data produced by the LCPE. The LCS determines whether a by combining this data with the actual carry signal that was received from the previous section. It is necessary to generate a local clock pulse for a specific higher-order bit. Consequently only the flip-flops that need to be toggled receive. clock pulses but the remaining flip-flops dont do anything. Power consumption and switching activity are further reduced by this selective clock distribution. The counter bits are stored in Toggle Flip-Flops (TFFs) which receive the generated local clock pulses. TFFs offer a straightforward and effective solution because a counter bit only needs to toggle when a legitimate clock pulse is generated. application. An UP control signal determines the direction of counting.

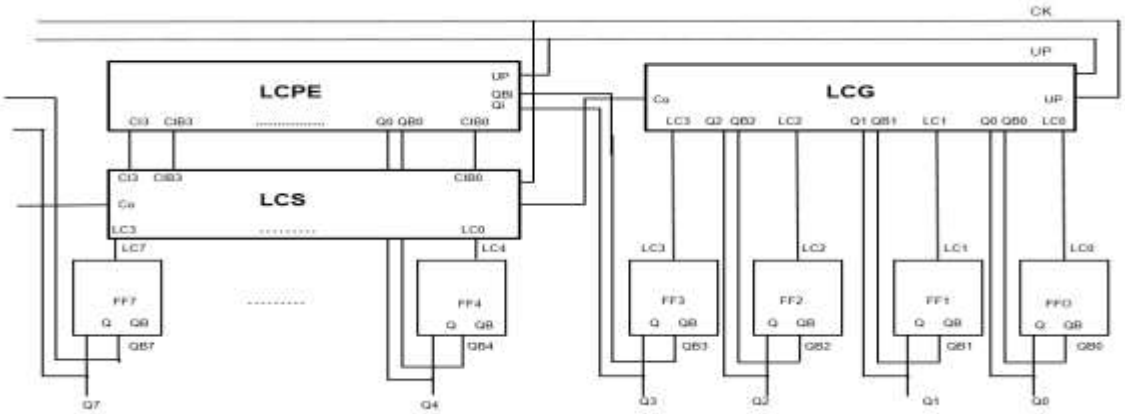

Fig 3.1: Complete architecture of proposed counter

When the UP signal is high, the counter performs incrementing operations, and when the UP signal is low, it performs decrementing operations. This functionality is achieved using multiplexers that select either the true outputs or complemented outputs of the counter bits. To further improve power efficiency, leakage reduction techniques such as the **LECTOR technique** in the LCG and the **stacking inverter technique** in the LCPE and LCS blocks are incorporated. These techniques reduce leakage current and static power dissipation while maintaining correct circuit operation. Thus, the proposed architecture combines local clock generation, carry pre-evaluation, selective clock distribution, and low-power design techniques to achieve a high-speed and energy-efficient synchronous up/down counter.

3.1 Local Clock Generator (LCG)

The Local Clock Generator is the first and most important block of the proposed counter. Rather than sending the global clock to each flip-flop its primary function is to produce local clock pulses for the lower-order bits. Every flip-flop in a traditional synchronous counter receives the clock signal during each clock cycle even if its output remains unchanged. This raises power consumption and results in needless switching activity.

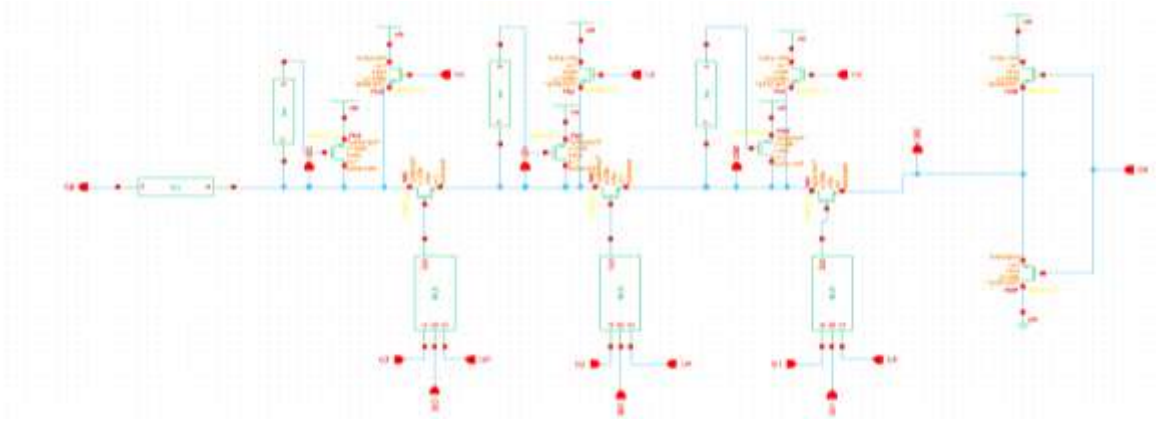

Fig 3.2: Cadence Schematic Implementation of LCG

The LCG only produces clock pulses when a bit needs to toggle in order to solve this issue. PMOS and NMOS transistors are used in a Manchester carry chain. A higher-order bit only toggles during up-counting when every lower-order bit is logic 1. . Only when every lower-order bit is logic 0 does a higher-order bit toggle during down-counting. Depending on the UP control signal multiplexers within the LCG choose between complemented outputs (QB) and true outputs (Q). Consequently up-counting and

down-counting operations can be carried out by the same hardware. The LCG consequently lowers dynamic power consumption increases efficiency and decreases clock activity.

3.2 Local Clock Pre-Evaluator (LCPE)

The Local Clock Pre-Evaluator is used for higher-order counter sections. In large counters, carry propagation from one stage to another introduces delay. Waiting for the carry signal to arrive can slow down the counting operation.To solve this issue, the LCPE predicts the carry condition before the actual carry arrives. It continuously monitors the present state of the counter bits and generates intermediate carry signals called CIB0, CIB1, CIB2, and CIB3.

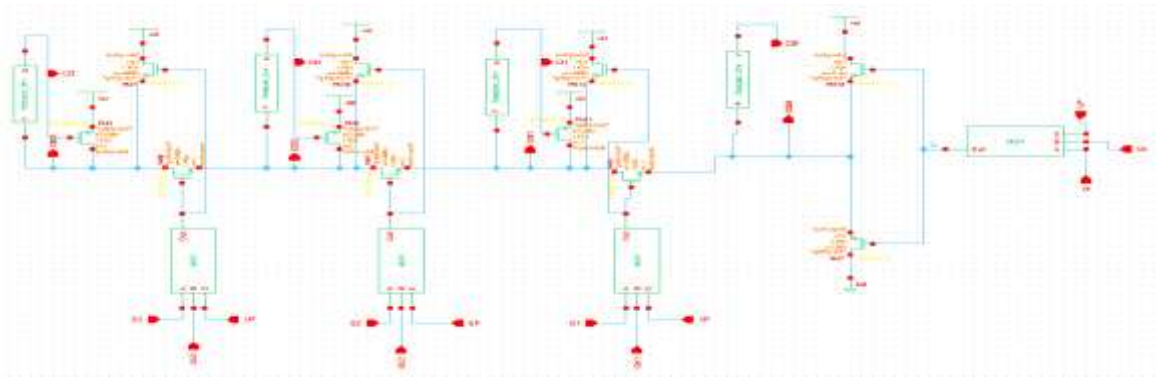

Fig 3.3: Cadence Schematic Implementation of LCPE

The LCPE operates in two phases:Precharge Phase: PMOS transistors charge the internal nodes to logic high.Evaluation Phase: NMOS transistors evaluate the selected counter-bit values and determine whether a carry condition is likely to occur. These pre-evaluated carry signals are stored and later sent to the Local Clock Selector. Since the carry information is already prepared before the actual carry arrives, the overall propagation delay is significantly reduced. This improves the speed of the counter

3.3 Local Clock Selector (LCS)

The Local Clock Selector (LCS) is a key component of the proposed synchronous up/down counter and serves as the final decision-making block for local clock generation It receives the pre-evaluated carry signals (CIB0-CIB3) produced by the Local Clock Pre-Evaluator (LCPE) as well as the actual carry input (Ci) from the lower-order counter section. The LCS decides whether a local clock pulse should actually be generated whereas the LCPE anticipates potential carry conditions beforehand. Unnecessary switching activity is avoided when the carry signal is inactive because no local clock pulse is generated and the corresponding flip-flops maintain their current states. The LCS only creates local clock pulses for the counter bits that need to be toggled when the carry signal becomes active. It does this by combining the carry information with the pre-evaluated signals. This selective clock distribution enhances overall counter performance and lowers dynamic power consumption. Domino logic or pass-transistor logic can be used to implement the LCS. While the domino-based LCS offers faster operation and lower propagation delay at the cost of slightly higher circuit complexity and area the pass-transistor-based LCS offers fewer transistors less area and lower power consumption. Therefore the particular power area and speed requirements of the design determine the implementation choice.

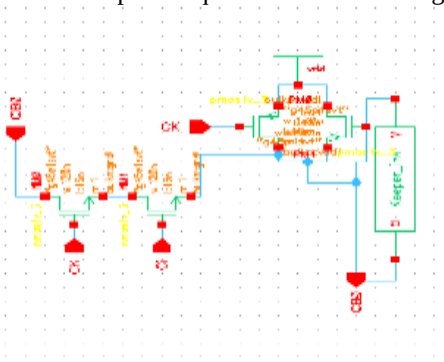

Fig 3.4: Cadence Schematic Implementation of LCS

3.4 Toggle Flip-Flop (TFF)

The Toggle Flip-Flop (TFF) serves as the storage element in the proposed synchronous up/down counter.Whenever a valid local clock pulse is received its main job is to store and update the counter state. A TFF automatically carries out the toggle operation required in counter applications in contrast to a D Flip-Flop which needs extra logic to determine the next state. The TFF shifts

from logic 0 to logic 1 or from logic 1 to logic 0 upon receiving a local clock pulse produced by the LCG or LCS. In the absence of a local clock pulse the flip-flop maintains its current state. The compact 16-transistor TFF architecture used in the suggested design aids in lowering power and area consumption while preserving dependable performance. Keeper transistors are also included to protect the stored data and stop undesired state changes brought on by noise or leakage currents.

3.5 LECTOR Technique

Fig 3.13 shows the transistor-level schematic of the LECTOR-based inverter used in the proposed design. The circuit is made up of two leakage control transistors (PM0 and NM1) and two conventional switching transistors (PM1 and NM0). The pull-up and pull-down networks are separated by the leakage control transistors to form a self-contained stacked structure. One of the leakage control transistors stays close to the cutoff region while it is operating which raises the effective resistance between VDD and ground and lowers subthreshold leakage current. The circuit is appropriate for low-power VLSI applications because it achieves much lower leakage power dissipation while performing the same logic inversion function as a traditional CMOS inverter. The transistor-level schematic of the LECTOR-based inverter used in the suggested design is displayed in Fig. 3. 13. Two PM0 and NM1 leakage control transistors and two PM1 and NM0 conventional switching transistors make up the circuit. A self-controlled stacked structure is produced by inserting the leakage control transistors between the pull-up and pull-down networks. One of the leakage control transistors stays close to the cutoff region while it is operating which raises the effective resistance between VDD and ground and lowers subthreshold leakage current. The circuit is appropriate for low-power VLSI applications since it achieves significantly lower leakage power dissipation while performing the same logic inversion function as a traditional CMOS inverter.

3.6 Stacking Inverter Technique

The stacking inverter technique is employed in the Local Clock Pre-Evaluator (LCPE) and Local Clock Selector (LCS) blocks to further reduce leakage power. Static power dissipation can occur in a traditional CMOS inverter when leakage current passes through the OFF transistors. By joining more transistors in series to create a stacked configuration the stacking technique alters the inverter structure. The effective threshold voltage rises and the gate-to-source voltage of the transistors decreases when several transistors in the stack are turned off at the same time. This phenomenon suppresses sub-threshold leakage current considerably. Additionally the series-connected transistors restrict undesired current flow by raising the resistance of the leakage path between VDD and GND. As a result the stacking inverter technique maintains the LCPE and LCS blocks functional performance while reducing static power consumption.

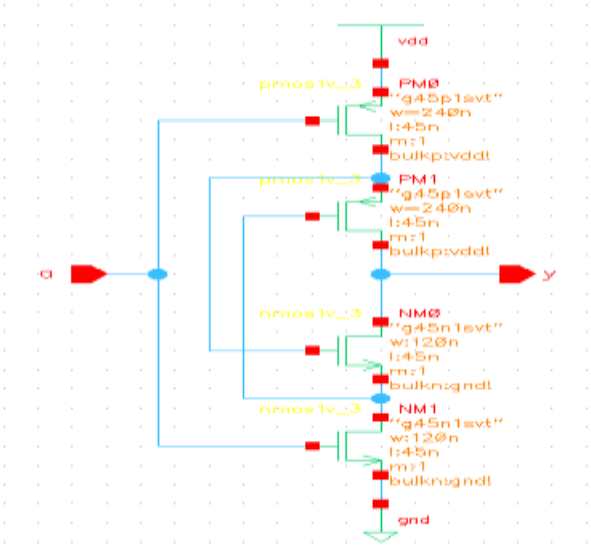

Fig 3:5: Cadence Schematic Implementation of Lector Technique

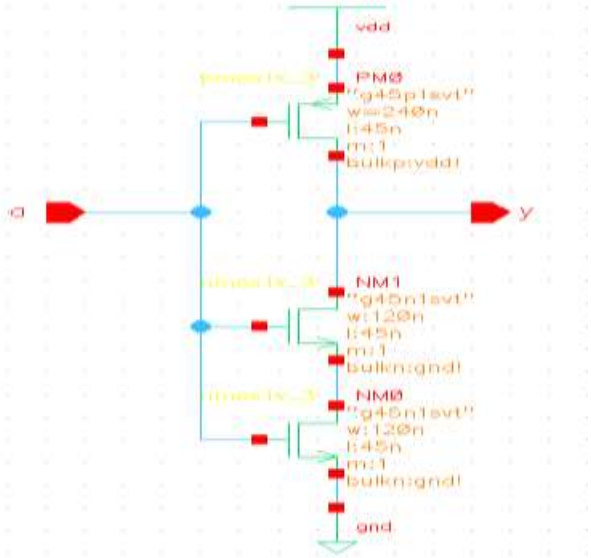

Fig 3:6: Cadence Schematic Implementation of Stacking Inverter Technique

3.7 Complete Counter Schematic

In order to minimize switching activity and eliminate needless clock transitions the LCG is in charge of producing local clock signals for the lower-order counter bits. The LECTOR technique is integrated into the LCG to minimize leakage power within the clock generation circuitry. By preventing undesired current flow between the power supply and ground the leakage control transistors increase energy efficiency.The LCPE and LCS blocks are used for the higher-order stages to assess carry conditions beforehand and produce the necessary local clock pulses only when needed. Stacking inverter structures are used in these blocks to further lower static power dissipation and leakage current. By ensuring that each flip-flop receives a clock signal only during legitimate state transitions this selective clock distribution mechanism improves power efficiency.The TFFs are driven by the generated local clocks which synchronously store and update the counter states.

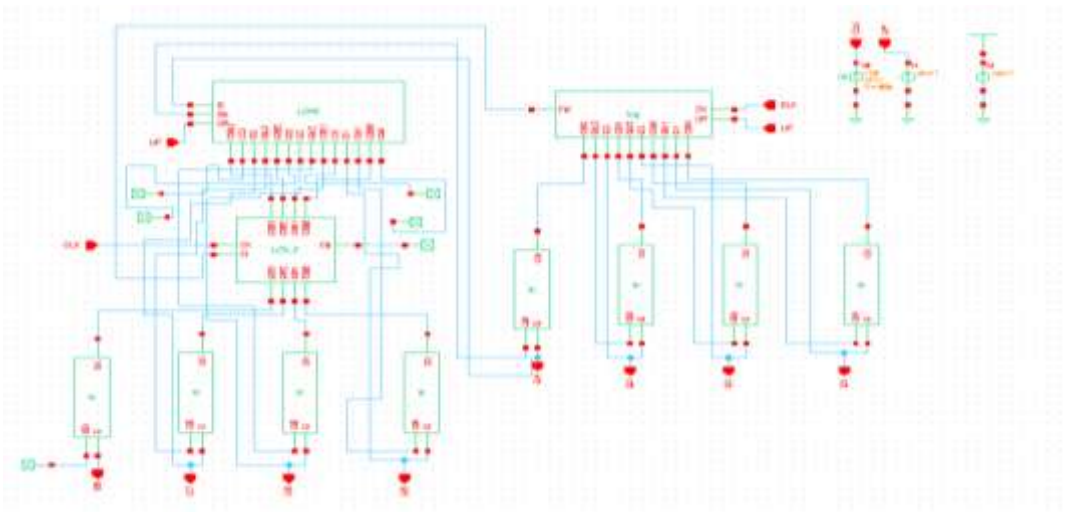

Fig 3.7: Complete Schematic of Proposed Synchronous Up/Down Counter

By choosing the true or complemented counter outputs within the clock-generation circuitry the UP control signal determines the counting direction. This allows for both up-counting and down-counting operations to be performed using the same hardware structure.An efficient low-power design strategy is produced by combining clock gating LECTOR-based leakage reduction stacking inverter techniques and local clock generation. Together these methods improve energy efficiency lower switching activity lower leakage current and lower power consumption without sacrificing the counters operational dependability.

IV. RESULTS AND DISCUSSION

4.1 Down-Counting Operation

Figure 4.1 shows the transient simulation waveform corresponding to down-counting operation. When the UP control signal is set to logic low, the counter decrements its count value sequentially at each valid clock cycle. The counter outputs follow the reverse binary sequence, such as 1111, 1110, 1101, 1100, and so forth. The waveform confirms that the counter correctly performs decrement operations without functional errors.The generated local clock signals and carry evaluation circuitry operate as intended, enabling reliable down-counting behavior.The simulation results obtained for both counting modes verify the correct operation of the proposed synchronous up/down counter. The counter successfully performs bidirectional counting while maintaining proper synchronization and reduced switching activity through the local clock generation architecture.

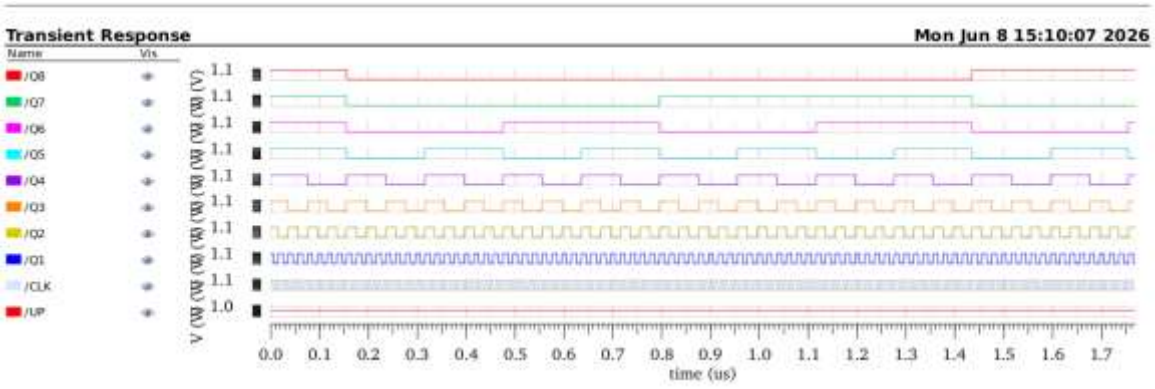

Fig 4.1: Transient waveform of the proposed synchronous down counter.

4.2 Up-Counting Operation

Figure 4.2 illustrates the waveform obtained during up-counting operation. When the UP control signal is maintained at logic high, the counter increments its count value sequentially with each valid clock cycle. The counter outputs transition in the binary sequence 0000, 0001, 0010, 0011, 0100, and so on. The waveform confirms that all counter bits are updated correctly according to the generated local clock signals. The observed output sequence verifies the successful implementation of the up-counting functionality and demonstrates proper synchronization among all counter stages.

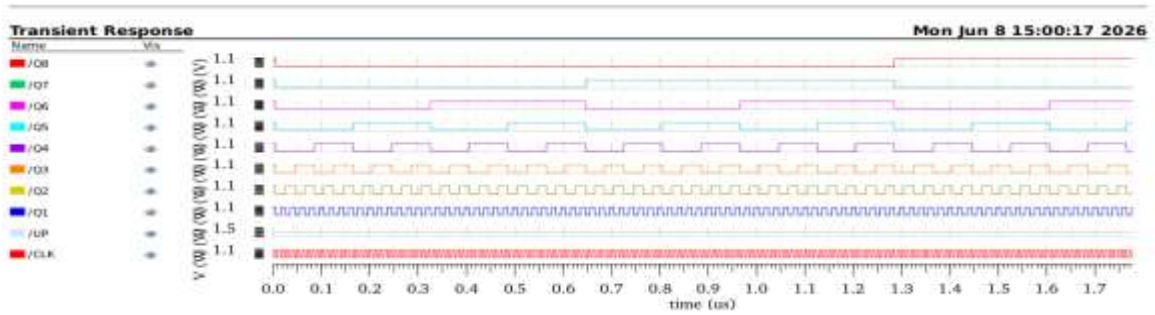

Fig 4.2: Transient waveform of the proposed synchronous up counter

The performance of the proposed synchronous counter was evaluated in Cadence Virtuoso through power and delay analysis under identical simulation conditions. The average power consumption of the existing counter architecture was measured as 83.15 µW, whereas the proposed counter consumed only 46.25 µW. This reduction was achieved through the incorporation of the LECTOR technique in the Local Clock Generator (LCG) and the stacking inverter technique in the Local Clock Pre-Evaluator (LCPE) and Local Clock Selector (LCS), which effectively suppress leakage current and minimize unnecessary power dissipation.

Table 4.1 Performance Comparison of Existing and Proposed Counter

Parameter	Existing Counter using clock-gated	Proposed Counter using LECTOR and Stacking Inverter	Percentage Improvement
Average Power Consumption (µW)	83.15	46.25	44.38% Improvement
Propagation Delay (ps)	93.46	87.92	5.93% Improvement
MOS Count	239	254	6.28% Increase

The percentage reduction in power consumption was calculated to be 44.38%, demonstrating a significant improvement in energy efficiency. In addition to power optimization, delay analysis was performed to evaluate the timing performance of the proposed design. The propagation delay of the existing counter was measured as 93.46 ps, while the proposed counter exhibited a reduced delay of 87.92 ps. The improvement in delay is attributed to the optimized local clock generation and carry evaluation mechanisms, which enable faster signal propagation through the counter. The percentage reduction in propagation delay was found to be 5.93%. These results confirm that the proposed counter architecture not only achieves substantial power savings but also improves timing performance, resulting in a high-speed and energy-efficient synchronous up/down counter.

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